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[54] **MEMORY EFFICIENT CHANNEL DECODING CIRCUITRY**

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[51] **Int. Cl.**[6] **H04B 1/38**; H04L 5/16

[52] **U.S. Cl.** **370/210**; 370/203; 375/219; 375/260; 375/232; 364/726.02; 364/726.03

[58] **Field of Search** 370/204, 205, 370/206, 208, 210, 244, 484; 375/245, 347, 362, 219, 232, 260, 302; 364/726.02, 726.03, 726.04

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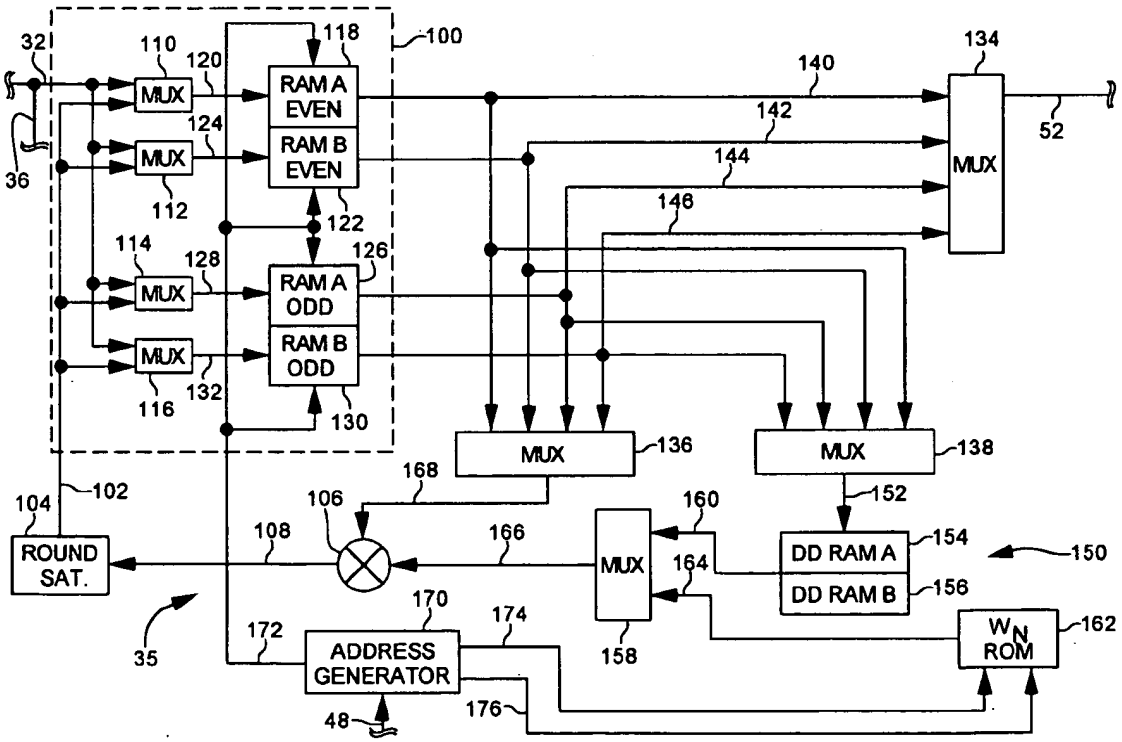
Primary Examiner—Chi H. Pham
Assistant Examiner—Frank Duong
Attorney, Agent, or Firm—JImmy L. Funke

[57] **ABSTRACT**

A memory efficient channel decoder circuit is provided for channel decoding differentially modulated data samples comprising multiple adjacent carriers each including two data samples associated therewith. The decoder circuit includes a pair of working read/write memory circuits partitioned into even and odd memory blocks, a separate read/write memory circuit connected thereto, and a complexmultiplier circuit having a first input connected to the working memory circuits, and a second input coupled to the separate read/write memory and a read only memory containing predefined calculation values. An in-place decimation-in-time FFT algorithm is used to differentially demodulate and frequency descramble (de-interleave) the data samples of each data symbol, as well as providing for automatic frequency control correction of the data samples.

12 Claims, 5 Drawing Sheets



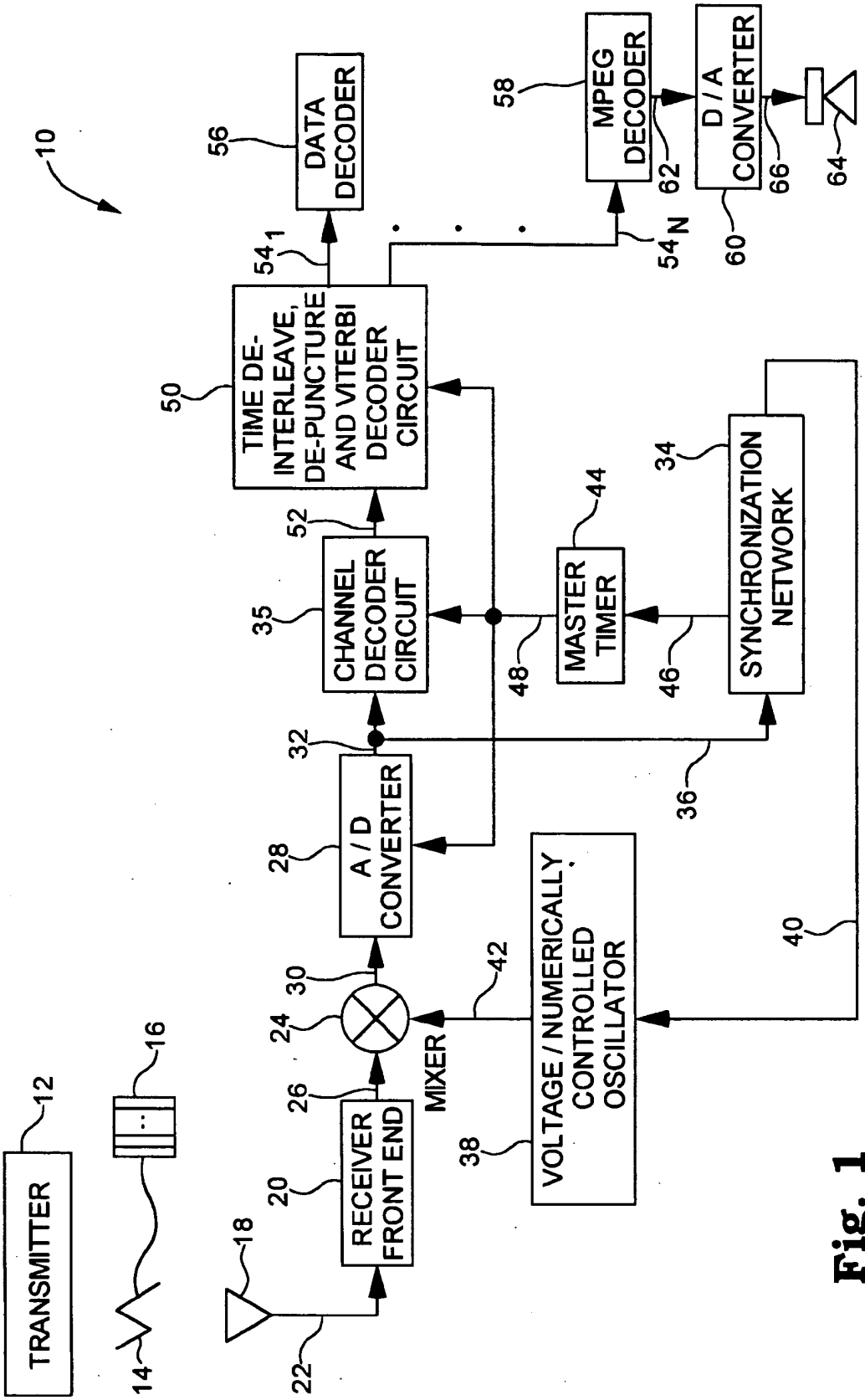

10
TRANSMITTER
12
14
16
18
20
RECEIVER FRONT END
22
24
26
MIXER
28
A / D CONVERTER
30
32
34
SYNCHRONIZATION NETWORK
35
CHANNEL DECODER CIRCUIT
36
38
VOLTAGE / NUMERICALLY CONTROLLED OSCILLATOR
40
42
44
MASTER TIMER
46
48
50
TIME DE-INTERLEAVE, DE-PUNCTURE AND VITERBI DECODER CIRCUIT
52
54 1
54 N
56
DATA DECODER
58
MPEG DECODER
60
62
D / A CONVERTER
64
66

Fig. 1

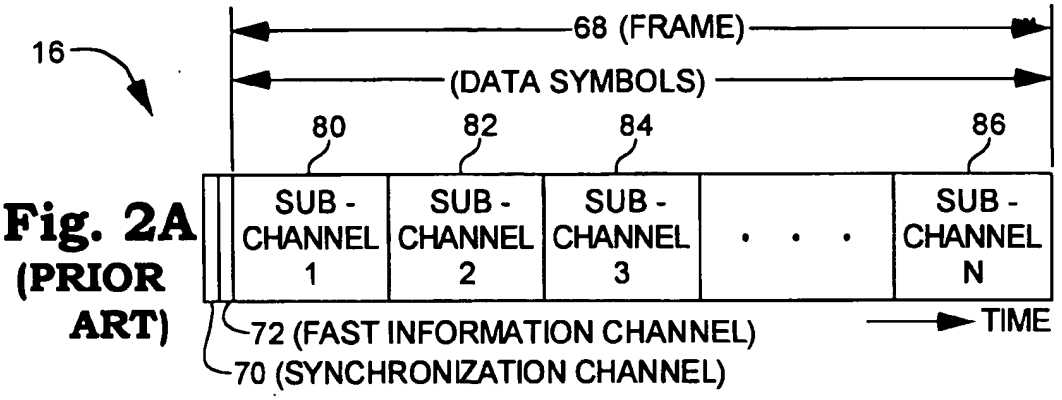


Fig. 2A (PRIOR ART)

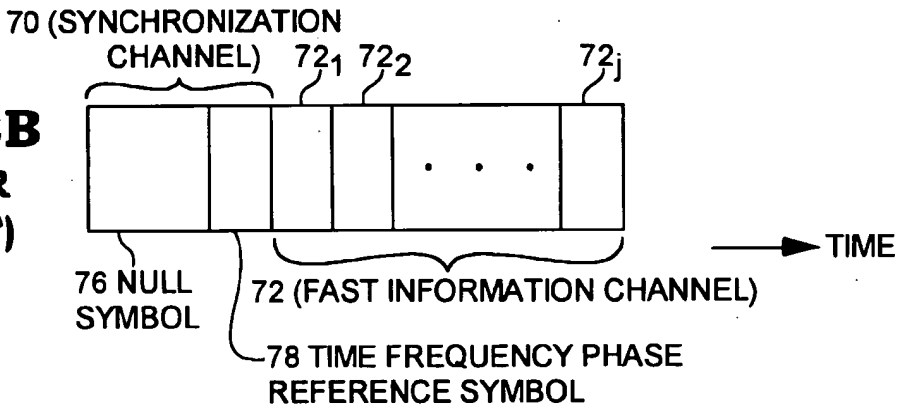


Fig. 2B (PRIOR ART)

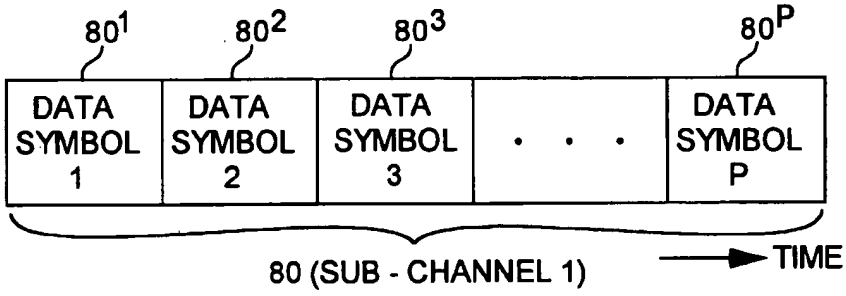


Fig. 2C (PRIOR ART)

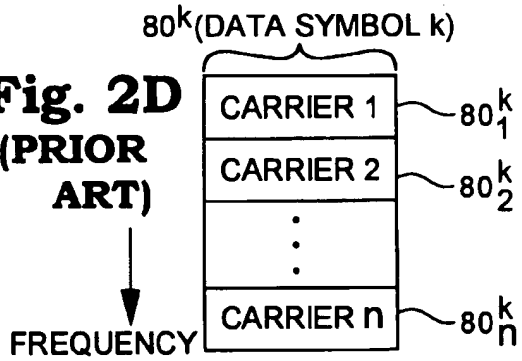


Fig. 2D (PRIOR ART)

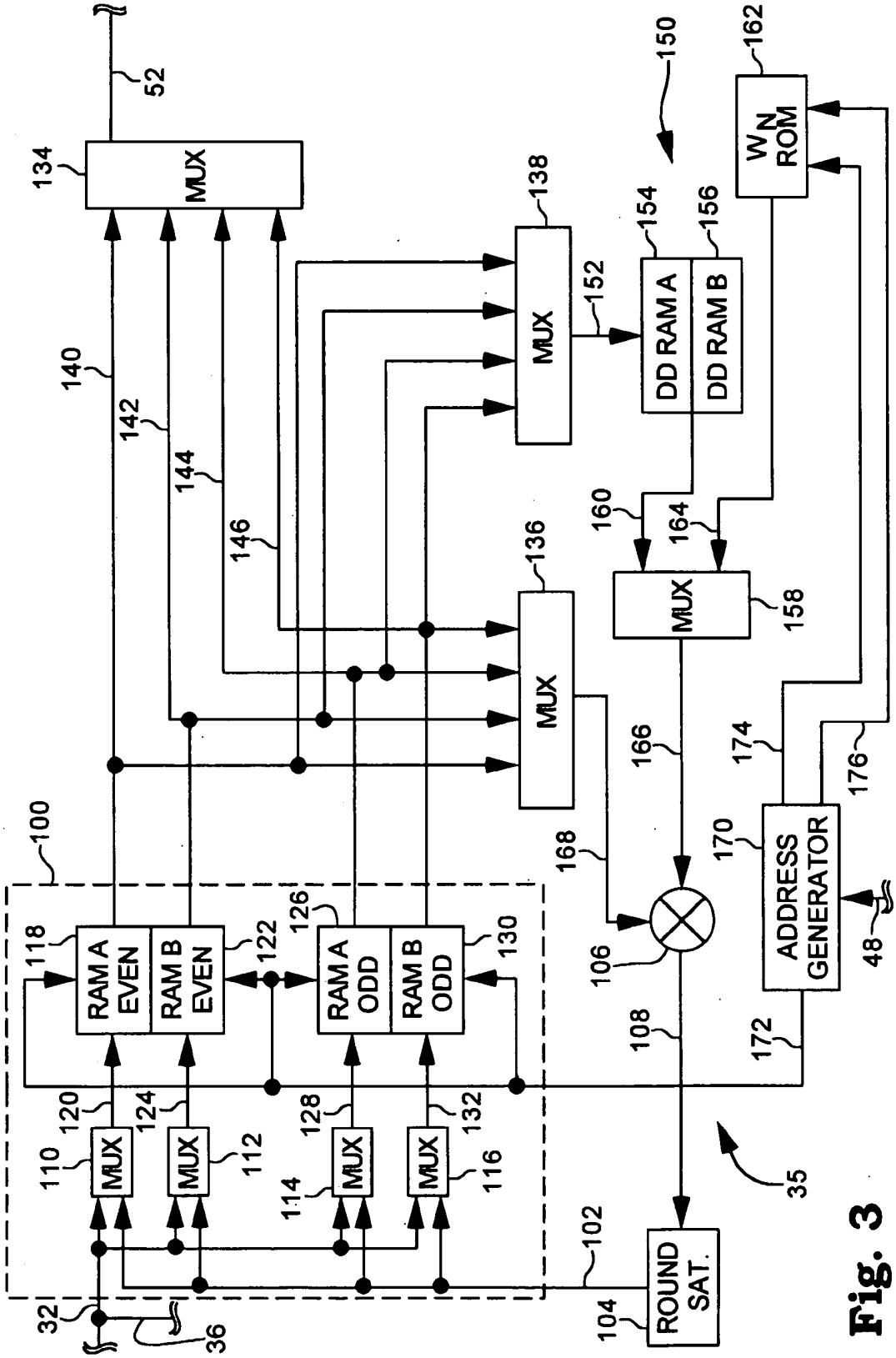

52
134
MUX
138
MUX
152
150
154
DD RAM A
156
DD RAM B
162
W_N ROM
140
142
144
146
136
MUX
160
164
MUX
158
166
174
176
168
170
ADDRESS GENERATOR
48
106
108
172
100
118
RAM A EVEN
RAM B EVEN
122
126
RAM A ODD
RAM B ODD
130
120
124
128
132
110
MUX
MUX
112
MUX
MUX
114
116
35
102
ROUND SAT.
104
32
36

Fig. 3

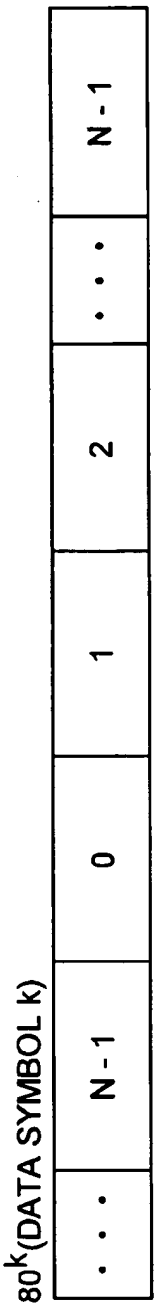


Fig. 4A

Fig. 4B

Fig. 4C

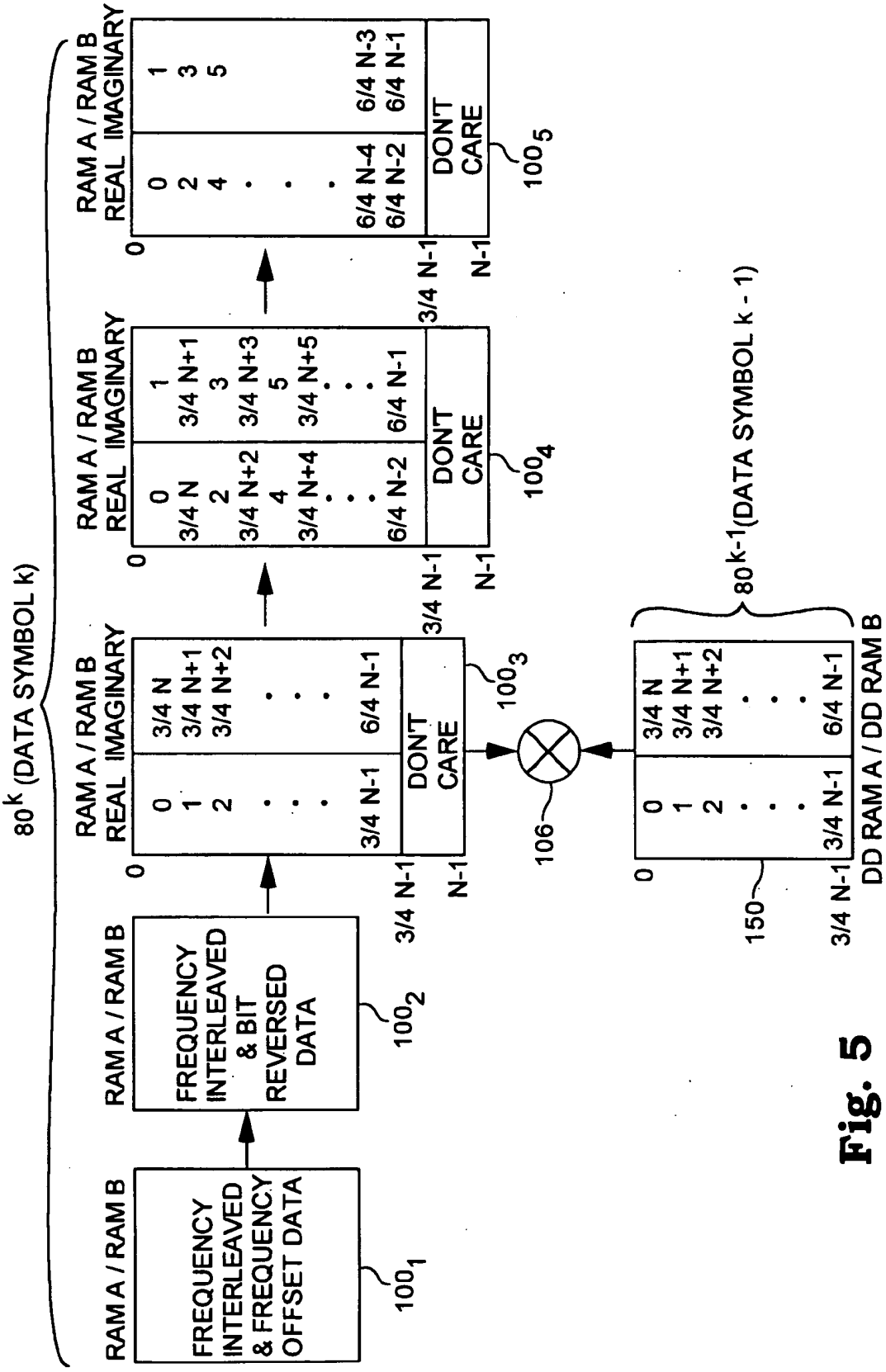

80^k (DATA SYMBOL k)
RAM A / RAM B
FREQUENCY INTERLEAVED & FREQUENCY OFFSET DATA
100_1
RAM A / RAM B
FREQUENCY INTERLEAVED & BIT REVERSED DATA
100_2
RAM A / RAM B REAL IMAGINARY
DON'T CARE
100_3
106
RAM A / RAM B REAL IMAGINARY
DON'T CARE
100_4
RAM A / RAM B REAL IMAGINARY
DON'T CARE
100_5
80^k-1 (DATA SYMBOL k - 1)
150
DD RAM A / DD RAM B

Fig. 5

MEMORY EFFICIENT CHANNEL DECODING CIRCUITRY

CROSS REFERENCE TO RELATED U.S. PATENT APPLICATIONS

The present invention relates to U.S. Ser. No. 08/823,917 which is related to a digital audio broadcasting (DAB) system and being filed concurrently with this invention.

FIELD OF THE INVENTION

The present invention relates generally to techniques for decoding and descrambling encoded data, and more specifically to such techniques for decoding and descrambling data including multiple carriers that are phase modulated over time.

BACKGROUND OF THE INVENTION

Digital techniques for the transmission and reception of sound information, sometimes referred to a digital audio broadcasting (DAB), have progressed over the past few years and are anticipated, on a worldwide basis, to replace the present frequency modulation (FM) method of transmitting audio and other information. Digital audio broadcasting (DAB) is not only anticipated to replace FM modulation, but the fidelity of audio signals transmitted and received by DAB systems will be greatly enhanced, making DAB's acceptance welcomed worldwide.

One such DAB technique, the Eureka-147 digital audio broadcasting system, has been accepted around the world as an excellent technical solution for digital sound broadcasting to the mobile environment. The Eureka-147 DAB standard ETS300401 specifies a digital transmission technique for satellite, terrestrial, and cable distribution of sound and data in accordance with the Eureka-147 format.

The Eureka-147 standard ETS300401 specifies a Coded-Orthogonal Frequency Division Multiplex (COFDM) modulation technique, wherein the digital information is transmitted in the complex frequency domain using $\pi/4$-shifted D-QPSK on each of multiple carriers with 2 bits per carrier. A transmitter of such a DAB signal is required by ETS300401 to use an Inverse Fast Fourier Transform (IFFT) to convert the signal from frequency to time prior to transmission thereof.

Referring now to FIGS. 2A–2D, the format of broadcast information, in accordance with the Eureka-147 ETS300401 standard, is shown. The digital information depicted in FIG. 2A is defined by frames of information, such as frame **68**. Frame **68** defines a structure having a juxtaposition arrangement that includes a synchronization channel **70** which occurs first in time in frame **68**, followed by a Fast Information Channel **72** (FIC), which is followed by sets of data symbols which are arranged as successive time multiplexed subchannels, sub-channel 1, sub-channel 2, sub-channel 3 . . . sub-channel N, shown respectively by blocks **80, 82, 84 . . . 86**.

The synchronization channel **70**, shown in FIG. **2B**, comprises symbols designated null symbol **76** and time frequency phase reference symbol (TFPR) **78**. FIC **72** includes a number of data symbols illustrated in FIG. **2B** as data symbols 72_1, 72_2, . . . 72_j. In accordance with the ETS300401 standard, the FIC **72** may include either three or eight such data symbols. The synchronization channel **70** is added at the beginning of each frame **68** to permit the receiver to synchronize, both in time and carrier frequency, with the stream of data symbols.

As seen in FIG. 2C, each of the sub-channels of data, such as sub-channel 1 (**80**), is further defined as containing multiple adjacent data symbols, data symbol 1, data symbol 2, data symbol 3, . . . data symbol p, respectively shown in blocks 80^1, 80^2, 80^3, and 80^p. With reference to FIG. **2D**, each data symbol within a particular sub-channel, such as the kth data symbol of sub-channel 1 (80^k), is further defined as containing multiple carriers, carrier 1, carrier 2, carrier 3, . . . carrier n, respectively shown in blocks 80^k_1, 80^k_2, and 80^k_n, wherein the n carriers are spread over a frequency bandwidth of interest. Each of the carriers are phase modulated between adjacent data symbols so that each carrier is phase modulated over time. Thus, each of the n carriers are transmitted simultaneously as a data symbol, and each of the p data symbols are transmitted at successive discrete time intervals.

Under standard ETS300401, the Eureka-147 system has the capability of operating in any of four operational modes, each including a different number of active carriers as set forth in Table 1 below. Since the transmitted information is encoded with two bits per carrier, the number of data points placed on each data symbol is equal to the number of carriers times two, thus defining the lengths of data vectors used to spread information across the frequency domain for each of the operational modes.

TABLE 1

Eureka-147 Operational modes				
	Mode 1	Mode 2	Mode 3	Mode 4
Number of Active Carriers	1536	384	192	768
Number of Data Vector Points	3072	768	384	1536

The $\pi/4$-Differential QPSK modulation technique conveys the information of interest in the rotation of each carrier's phase with respect to the previous symbol's corresponding carrier phase. The phase rotation applied to each carrier is determined by the next two bits to be placed onto that carrier. The data vectors applied to the data symbols 66 are further pre-scrambled before being applied to the carriers, wherein this process of pre-scrambling is known in the art as frequency interleaving. Finally, the ETS300401 standard allows for transmission of data at different rates so that the sub-channels **80–86** are time-multiplexed and are previously pre-scrambled in time, wherein this process of pre-scrambling is known in the art as time interleaving.

A DAB receiver must be capable of receiving the transmitted signals described hereinabove, synchronize with such signals in both time and carrier frequency, and decode the signals for replication of the original information. Decoding of the information in a Eureka-147 based DAB receiver requires the capability of performing a complex Fast Fourier Transform (FFT) to reverse the effect of the IFFT applied by the Eureka-147 DAB transmitter. Due to the four operational modes of the Eureka-147 system as set forth in Table 1 above, a Eureka-147 based DAB receiver must correspondingly be capable of performing various length FFTs as set forth in Table 2 below. It should be understood that, under ETS300401, Table 1 sets forth only the number of active carriers per mode, and that such active carriers make up only ¾ of the total number of carriers for each mode. Table 2 thus sets forth the FFT length requirements for decoding the total number of carriers, N, for each mode of operation of the

Eureka-147 system. It can thus be seen from Table 2 that a Eureka-147 based DAB receiver must have the capability to perform complex Fast Fourier Transforms of lengths 2048, 1024, 512 and 256 for each of modes 1, 4, 2 and 3 respectively.

TABLE 2

Complex N	Potential Data Vector Points	Active Carrier Multiplier	Number of Data Vector Points	Operations 1 Mode
2048	4096	3/4	3072	1
1024	2048	3/4	1536	4
512	1028	3/4	768	2
256	512	3/4	384	3

Eureka-147 based DAB information is time and frequency interleaved prior to broadcast thereof in accordance with a complex IFFT process. In channel decoding and frequency de-interleaving (descrambling) such signals, known Eureka-147 based receiver systems utilize an arrangement of N-capacity inputs and output data storage buffers operable to store the N-carrier information prior to and following the FFT process. Within the FFT process itself, such known prior art systems further require two more N-capacity memory units for carrying out the FFT process and a fifth N-capacity memory unit for holding previous symbol values for the channel decoding process. Known prior art system thus require a total of 5N storage locations for decoding N-carrier Eureka-147 based DAB information.

Such prior art Eureka-147 based DAB receiving systems are expensive in terms of memory usage required for management thereof. What is therefore needed is an efficient technique for channel decoding and de-interleaving (descrambling) broadcast Eureka-147 based DAB information which minimizes memory required therefore.

SUMMARY OF THE INVENTION

The channel decoding circuitry of the present invention addresses the needs and concerns set forth in the BACKGROUND section. In accordance with one aspect of the present invention, channel decoding circuitry comprises a first memory circuit having a first input for receiving and storing therein channel encoded digital data, a second input for receiving channel decoded digital data, and an output for producing the channel decoded digital data. The channel encoded digital data is defined by a number of data symbols each including multiple adjacent data carriers phase modulated over time. A second memory circuit holds channel encoded digital data of a previous data symbol therein and has an input coupled to the first memory circuit output and an output. A third memory circuit provides predefined calculation values at an output thereof. A multiplier circuit has a first input coupled to the first memory circuit output, a second input coupled to the second memory circuit output and to the third memory circuit output, and an output coupled to the second input of the first memory circuit. The multiplier circuit produces channel decoded digital data by complex multiplying corresponding data carriers provided by the first and second memory circuits along with the predefined calculation values provided by the third memory circuit. The first memory circuit simultaneously stores channel decoded data of a present data symbol provided by the multiplier circuit, produces channel decoded digital data of a previous data symbol at the first memory circuit output and replaces the channel decoded digital data of the previous data symbol with channel encoded digital data of a next data symbol.

In accordance with another aspect of the present invention, the multiplier circuit further corrects for frequency offsets between data carrier frequencies of the encoded digital data and corresponding actual data carrier frequencies thereof by complex multiplying data carriers provided by the first memory circuit with the predefined calculation values.

One object of the present invention is to provide a memory efficient channel decoder that significantly reduces memory requirements over conventional channel decoders.

Another object of the present invention is to provide such a channel decoder that further provides for automatic frequency control and frequency de-interleaving.

Yet another object of the present invention is to provide such a memory efficient channel decoder that provides for automatic frequency control, channel decoding and frequency descrambling utilizing only a single complex multiplier circuit.

These and other objects of the present invention will become more apparent from the following description of the preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of one embodiment of a broadcast data receiver particularly suited for reception of COFDM modulated data, incorporating a channel decoder in accordance with the present invention.

FIG. 2 is composed of FIGS. 2A, 2B, 2C and 2D and illustrates a known frame structure of the digital information transmitted by the transmitter of FIG. 1 and received by the receiver of FIG. 1.

FIG. 3 is a block diagram illustrating one embodiment of a channel decoding circuit particularly suited for decoding multiple carrier phase modulated digital data, in accordance with the present invention.

FIG. 4 is composed of FIGS. 4A–4C and illustrates a preferred technique of utilizing multiple memory banks for accomplishing digital data decoding in accordance with the present invention.

FIG. 5 is a diagrammatic illustration of the contents of the memory circuits of FIG. 3 throughout the channel decoding, frequency descrambling and automatic frequency control processes of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

For the purposes of promoting an understanding of the principles of the invention, reference will now be made to the embodiment illustrated in the drawings and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, such alterations and further modifications in the illustrated device, and such further applications of the principles of the invention as illustrated therein being contemplated as would normally occur to one skilled in the art to which the invention relates.

The Eureka-147 system utilizes multiple frequency domain carriers as vehicles for digital information, rather than a single-phase carrier having a high data rate as is known in the prior art. The use of the multiple carriers to transmit digital information in the form of digital pulses increases data symbol duration as to avoid intersymbol interference associated with delay spread of an RF channel. The wide bandwidth reduces the effects of narrow band multipath interference.

As discussed in the BACKGROUND section, the digital information carried by each of the multiple carriers is transmitted in the complex frequency domain using a p/4-differential quad-phase shift key (p/4-DQPSK) modulation scheme known as Coded-Orthogonal Frequency Division Multiplex, or COFDM, modulation. Each of the multiple carriers of the Eureka-147 system yields two bits of digital information via p/4 DQPSK modulation, and the multiple carriers are arranged in adjacent arrays using an inverse fast Fourier transform (IFFT) algorithm, which assigns complex phases to each frequency domain carrier. The data carried by the carriers are differentially encoded between individual carriers on successive symbols so that channel decoding thereof requires a differential demodulation process to be carried out by the digital information receiver. As is known in the art, such differential decoding techniques do not require synchronous demodulation, and precisely accurate bit timing with the incoming digital information is therefore not required because the differential decoding techniques used by the present invention eliminates errors associated with bit offset timing. The timing of the samples taken by the receiving elements of the Eureka-147 system thus need not be at the peak location of the "open eye" as is common in digital communication systems, but rather timing need only accurately reflect the beginning of a transmitted symbol. The bit timing of the present invention need only be approximately accurate to obtain a majority of the transmitted data, sometimes referred to as symbol energy.

Referring now to FIG. **1**, one embodiment of a broadcast data receiver **10**, particularly suited for reception of COFDM modulated data, is shown. Receiver **10** includes a known transmitter **12**, operable to transmit a digital data stream **14**, such as COFDM modulated data **16**, which is received by antenna **18**. Antenna **18**, in turn, routes the received information to a known receiver front end **20** via signal path **22**. The receiver front end **20** may have amplifying means to amplify the received signals as is known in the art, and routes such received/amplified signals to a known mixer **24** by way of signal path **26**. The mixer **24**, in response to the information signal provided thereto via signal path **26** and a feedback signal provided thereto by a known voltage/numerically controlled oscillator **38** via signal path **42**, combines these input signals and develops an output signal whose frequency is roughly equal to the difference between the frequencies of its input signals, and routes such an output signal to a known A/D converter **28** by way of signal path **30**. Mixer **24** thus provides a frequency-adjusted analog signal that is routed to the A/D converter **28**. The digital quantities generated by the A/D converter **28** are routed, by way of signal path **32**, to the channel decoder circuit **35** of the present invention, and to a known synchronization network **34** via signal path **36**. Channel decoder circuit **35**, in turn, provides a channel decoded signal to time de-interleave, de-puncture and viterbi decoder circuit **50** via signal path **52**. The channel decoded signal provided by channel decoder circuit **35** consists of multiplexed input time samples, representing in-phase and quadrature time components, and output soft-decision metrics representing the decoded frequency domain samples in time correct order to enter a time de-interleave, de-puncture and viterbi decoding process within time de-interleave, de-puncture and viterbi decoder circuit **50**. A preferred embodiment of such a circuit **50** is described in related Attorney Docket No. H-197792, and entitled MEMORY EFFICIENT TIME DE-INTERLEAVE, DE-PUNCTURE AND VITERBI DECODER CIRCUITRY, which is assigned to the assignee of the present invention, and which patent application is herein incorporated by reference.

Synchronization network **34** provides a signal synchronization signal to voltage/numerically controlled oscillator **38** via signal path **40**, and further provides a timing signal to a known master timer **44** via signal path **46**. The master timer **44**, sometimes referred to as a master clock, by means of its output signal on signal path **48** controls the sample timing by which all of the interconnected elements, such as A/D converter **28**, channel decoder circuit **35** and time de-interleave, de-puncture and viterbi decoder circuit **50**, sample their associated signals. In operation, the feedback loop established between A/D converter **28** and mixer **24**, by way of synchronization network **34** and voltage/numerically controlled oscillator **38**, synchronizes receiver **10** with the received signal **14** both in time and in frequency. Master timer **44** is responsive to the timing signal provided thereto by synchronization network **34** to produce the master timing signal on signal path **48**. The A/D converter **28**, channel decoder circuit **35** and time de-interleave, de-puncture and viterbi decoder circuit **50** are, in turn, responsive to the master timing signal on signal path **48** to process the received signal **14** in a time-synchronized manner.

The synchronization network **34** and voltage/numerically controlled oscillator **38** are responsive to the signal provided thereto via signal path **36** to acquire a "rough" frequency synchronization with the received signal **14**. Such an arrangement permits the receiver **10** to achieve a frequency lock of within a few carriers of the transmitted signal's frequency. The ETS300401 standard, however, requires a frequency lock of better than the frequency spacing between each of the multiple carriers, which translates to a frequency lock requirement of better than 0.02* carrier spacing. As will be discussed in greater detail hereinafter, the channel decoder circuit **35** of the present invention is operable to improve the frequency synchronization, in accordance with digital automatic frequency control (AFC) techniques, to achieve a frequency lock with the transmitted signal of better than 0.02* carrier spacing as required for data reliability.

The time de-interleave, de-puncture and viterbi decoder circuit **50** provides a number N of digital signals on signal paths 54_1–54_N, wherein N corresponds to the number of decoded channels of information. The decoded information available on any given signal path 54_K may be either music information or other digital data. If the decoded information is digital data other than music, the signal path is routed to a data decoder **56**, such as illustrated by signal path 54_1 in FIG. 1. If, however, the decoded information is music information, such as that present on signal path 54_N, the signal path is routed to an MPEG decoder **58** of known construction. The MPEG decoder **58** is connected to a D/A converter **60** via signal path **62**, and the D/A converter **60**, in turn, provides an analog output signal to speaker **64** via signal path **66** for audio reproduction of the transmitted signal.

Referring now to FIG. **3**, a preferred embodiment of a channel decoder circuit **35**, in accordance with the present invention, is shown. Central to channel decoder circuit **35** is a memory circuit **100** having a first input connected to signal path **32** and a second input connected to a rounding saturation circuit **104** via signal path **102**. Memory circuit **100** produces an output signal on a number of output signal paths **140–146**, which signal paths are multiplexed to single output lines **52**, **168** and **152** via known 4:1 multiplexing circuits (MUX) **134**, **136** and **138** respectively.

In one embodiment, memory circuit **100** includes four 2:1 multiplexing circuits (MUX) **110**, **112**, **114** and **116** of known construction, wherein each multiplexing circuit

110–116 has a first input connected to signal path 32 and a second input connected to signal path 102. Memory circuit 100 is partitioned into a pair of memory subcircuits RAM A and RAM B, each of which are further partitioned into RAM A EVEN 118 and RAM A ODD 126 circuits and RAM B EVEN 122 and RAM B ODD 130 circuits respectively. Preferably, memory circuits 118, 122, 126 and 130 are suitably partitioned from a single memory block, although the present invention contemplates providing such memory circuits from separate, or stand-alone, memory circuits. In either case, memory circuits 118, 122, 126 and 130 are temporary read/write storage circuits such as Random Access Memory (RAM) circuits of known construction.

RAM A EVEN 118 has an input connected to MUX 110 via signal path 120, and an output connected to first inputs of MUXs 134, 136 and 138 via signal path 140. RAM B EVEN 122 has an input connected to MUX 112 via signal path 124, and an output connected to second inputs of MUXs 134, 136 and 138 via signal path 142. RAM A ODD 126 has an input connected to MUX 114 via signal path 128, and an output connected to third inputs of MUXs 134, 136 and 138 via signal path 144. RAM B ODD 130 has an input connected to MUX 116 via signal path 132, and an output connected to fourth inputs of MUXs 134, 136 and 138 via signal path 146.

MUX 138 has an output connected to an input of a differential demodulation memory circuit 150 via signal path 152. In one embodiment, differential demodulation memory circuit 150 is partitioned into a DDRAM A memory circuit 154 and a DDRAM B memory 156. As with memory circuits 118, 122, 126 and 130, memory circuits DDRAM A 154 and DDRAM B 156 are preferably partitioned from a single memory block, although the present invention contemplates providing such memory circuits from separate, or stand-alone, memory circuits. In either case, memory circuits 154 and 156 are temporary read/write storage circuits such as Random Access Memory (RAM) circuits of known construction. Memory circuit 150 has an output connected to a first input of a known 2:1 multiplexing circuit (MUX) 158 via signal path 160.

Channel decoder circuit 35 further includes a memory circuit 162 connected to MUX 158 via signal path 164. Memory circuit 162 holds predefined calculation values therein, as will be discussed more fully hereinafter, and may therefore be a read-only-memory (ROM) circuit of known construction. Memory circuit 162 includes two address inputs connected to an address generator circuit 170 via signal paths 174 and 176. Address generator 170 is further connected to address inputs of RAM A EVEN 118, RAM B EVEN 122, RAM A ODD 126 and RAM B ODD 130 via signal path 172.

MUX circuit 158 includes a MUX output 166 connected to a first input of a complex multiplier circuit 106 which may be of known construction. A second input of complex multiplier circuit 106 is connected to a MUX output of MUX circuit 136. An output of complex multiplier circuit 106 is connected to an input of rounding saturation circuit 104 via signal path 108.

The channel decoder circuit 35 of the present invention is operable to channel decode the stream of digital data 14 by processing the digital data in accordance with a complex Fast Fourier Transform (FFT) of length 2048, 1024, 512 or 256, depending upon the operational mode of the Eureka-147 system as set forth in Table 2 above. For lengths 1024 and 256, a radix-4 in-place calculation is preferably used, and for lengths 2048 and 512, a split radix4–radix2 in-place calculation is preferably used. The channel decoder circuit 35 is also operable to perform frequency interleave descrambling as well as automatic frequency control (AFC) adjustments so that the resulting channel decoded digital signal provided by channel decoder circuit 35 on signal path 52 is in time correct order and is suitably adjusted in frequency to correct for any resulting offset between the transmitter 12 and receiver local oscillator 38. For all operational modes, the FFT is preferably calculated using a known decimation-in-time (DIT) algorithm which allows for an efficient use of hardware to accomplish both the decoding and descrambling processes, as well as the AFC correction process, as will be described more fully hereinafter.

With reference to FIGS. 1–4C, memory efficient operation of the channel decoder circuit 35 will now be described. With each new data symbol (see FIGS. 2A–2D) entering the receiver 10, the synchronization network 34 sends a timing signal to master timer 44. Master timer 44, in turn, produces a data enable signal on signal path 48 that resets the address generator 170. Thus, for every new data symbol entering circuit 35, the address generator 170 resets an address count on signal path 172 to an initial value, such as zero, and thereafter proceeds to count at a predefined clock rate.

Memory circuit 100 is partitioned into even and odd ram banks such that are two sets of even and odd banks, RAM A EVEN 118, RAM A ODD 1126 and RAM B EVEN 122, RAM B ODD 130. The manner in which the symbol's digital data (two bits per carrier) is input into the memory circuit 100 is determined in accordance with the value of the signal present on signal path 172. In one preferred embodiment, the digital data is directed into the respective even and odd ram banks by counting the number of ones in the address. If the number of ones in the address is even, the first data value of the present carrier is stored in RAM A EVEN 118. If, on the other hand, the number of ones in the address is odd, the first data value of the present carrier is stored in RAM A ODD 126. It should be understood that for an N-carrier system (see Table 2), each of the RAM A and RAM B memory banks must be of size N/2 to capture all of the encoded data.

As will be described in greater detail hereinafter, channel decoder circuit 35 is operable to compute an in-place Fast Fourier Transform, in accordance with a known decimation-in-time radix-4 or split radix4–radix2 algorithm, in order to simultaneously accomplish AFC correction and differentially demodulate as well as descramble (frequency de-interleave) the digital data. In so doing, the complex multiplier circuit 106 is operable to systematically complex multiply pairs of digital data from a present data symbol taken from either RAM A EVEN 118 and RAM A ODD 126, or RAM B EVEN 122 and RAM B ODD 130, with either corresponding digital data of the previous symbol stored in DDRAM A 154 and DDRAM B 156 during processing of the previous symbol and/or predefined calculation values taken from memory circuit 162. In accordance with either the radix-4 or split radix4–radix2 algorithms, four such multiplications must be performed per FFT butterfly as is known in the art. The output of the complex multiplier circuit 106 for any such multiplication is provided to rounding saturation circuit 104 in order to round and saturate the complex multiply results as is known in the art, and is thereafter provided back to memory circuit 100 via MUXs 110–116.

In accordance with an important aspect of the present invention, some data symbols are moved through one ram bank (RAM A EVEN/ODD or RAM B EVEN/ODD) while complex multiplications are performed on other data sym-

bols. Since the final output data pairs of the complex multiplication process are in time correct order, the input/output data pairs during the computation process can be exchanged one-for-one in the memory circuit **100**. Such a one-for-one exchange procedure eliminates any need for separate input and/or output data buffers which are used in prior art circuits as discussed hereinabove. Referring to FIGS. **4A–4C**, an example of the foregoing data flow process through channel decoder circuit **35** is shown.

FIG. **4A** illustrates the processing of the encoded digital data by channel decoder circuit **35** on a symbol-by-symbol basis. As illustrated in FIGS. **4B** and **4C**, as encoded data values for a present data symbol are withdrawn from one ram bank for decoding thereof via the FFT process, the opposite ram bank is simultaneously outputting decoded data values for the previous symbol(onto signal path **52**) and inputting encoded data values for the next data symbol via MUXs **110–116**). As discussed hereinabove, the data pairs for any given symbol are preferably moved through the ram banks on a one-for-one exchange basis.

Referring now to FIG. **5**, the contents of the ram banks of memory circuit **100** during the processing of any given data symbol, such as data symbol 68^k, during the various stages of the FFT algorithm, are illustrated. Upon detection of a symbol enable signal, circuit **35** loads the encoded symbol; i.e. frequency scrambled (interleaved) and frequency offset data symbol 68^k, into the ram banks of memory circuit $\mathbf{100}_1$ according to techniques described hereinabove. For the first complex multiply performed by complex multiplier **106** in the FFT process, the present invention takes advantage of the fact that the so-called FFT twiddle values forming some of the predefined calculation values stored in memory circuit **162** are all real valued (i.e., w(0)=1+j0). Address generator **170** provides first predefined addressing values to memory circuit **162** via circuit path **174**, to which circuit **162** is responsive to supply such twiddle values to MUX **158**. MUX **158**, in turn, supplies the twiddle values to complex multiplier circuit **106** as is known in the art. Address generator **170** further provides second predefined addressing values to memory circuit **162** during this first stage of FFT computation, to which circuit **162** is responsive to supply accumulated phase rotation values forming some of the predefined calculation values stored therein to MUX **158**. Since a decimation-in-time algorithm is used for the FFT, and the twiddle values for the first FFT stage are all real-valued, the AFC correction calculation can be made by the complex multiplier **106** using the digital data symbol values, the twiddle values and accumulated phase rotation values to correct frequency offset of the data symbol samples as is known in the art. The complex rotation of the time samples is accomplished using the same complex multiplier and twiddle rom memory circuit **162** required for the FFT computation, thus minimizing the hardware required to accommodate an AFC function. As required by the ETS300401 standard, frequency offset correction is performed during this first stage of FFT computation to ensure a frequency lock of better than 0.02* carrier spacing.

The second stage of the FFT algorithm accomplishes a first frequency descrambling (frequency de-interleaving) of the data symbol samples as shown by memory circuit $\mathbf{100}_2$. This first frequency descrambling in an in-place combined descramble that corrects for the bit-reversed nature of the FFT algorithm and frequency scrambling. As shown by memory circuit $\mathbf{100}_2$, the active carrier data points of the data symbol are placed in the upper portions of the even and odd memory banks RAM A and RAM B (**118–130**) which effectively reduces the amount of memory required to store the previous symbol's data points in the DDRAM A and DDRAM B memory circuit **150** as will be described more fully with respect to memory circuit $\mathbf{100}_3$. The second complex multiplication carried out by complex multiplier **106** thus places the symbol's data samples in time corrected order, as shown by the resultant memory circuit $\mathbf{100}_3$, beginning with data samples 0–3N/4–1 placed in the real locations, followed by data samples 3N/4–6N/4–1 placed in the imaginary locations, of the RAM A (RAM A EVEN **118** and RAM A ODD **126**) or the RAM B (RAM B EVEN **122** and RAM B ODD **130**) memory block, depending upon which of the ram banks is involved in the computation. The remaining locations of the EVEN and ODD ram banks are don't care conditions and correspond to the inactive carriers of the N-carrier system.

The third stage of the FFT algorithm accomplishes the differential demodulation process which takes two complex data samples at a time from each of the differential rams, DDRAM A **152** and DDRAM B **154**, and complex multiplies these data samples with corresponding data samples from either the RAM A (RAM A EVEN **118** and RAM A ODD **126**) or the RAM B (RAM B EVEN **122** and RAM B ODD **130**) memory block, depending upon which of the ram banks is involved in the computation as described hereinabove with respect to FIGS. **4A–4C**. This process is illustrated in FIG. **5** with respect to the contents of memory circuit $\mathbf{100}_3$ and memory circuit **150**. In preparation for the final descrambling stage of the FFT algorithm, the data samples resulting from the differential demodulation process are reordered before placing them back into the working ram memory bank (memory circuit **100**). As shown in the resultant contents of memory circuit $\mathbf{100}_4$, a preferred technique for reordering the demodulated data samples involves swapping the imaginary data points of the EVEN ram bank data samples with the real data points of the ODD ram bank data samples prior to placing the data points back into the working ram memory bank. The third complex multiplication carried out by complex multiplier **106** thus reorders the symbol's demodulated data samples, as shown by the resultant memory circuit $\mathbf{100}_4$, such that data samples 0, 3N/4, 2, 3N/4+2, 4, 3N/4+4 and so on are placed in the real locations, followed by data samples 1, 3N/4+1, 3, 3N/4+3, 5, 3N/4+5 and so on being placed in the imaginary locations, of the RAM A (RAM A EVEN **118** and RAM A ODD **126**) or the RAM B (RAM B EVEN **122** and RAM B ODD **130**) memory block, depending upon which of the ram banks is involved in the computation. The remaining locations of the EVEN and ODD ram banks are don't care conditions and correspond to the inactive carriers of the N-carrier system.

As illustrated by the DDRAM memory circuit **150** connected to the complex multiplier circuit **106** below the memory circuit $\mathbf{100}_3$ in FIG. **5**, only the data corresponding to the active carriers (see Table 1) need be stored therein. DDRAM A **152** and DDRAM B **154** each therefore need only be of size 3N/8 to thereby hold 3N/4 values of the active carriers (see Tables 1 and 2). This results in a significant savings in memory over known prior art systems. It is to be understood that during stage 3 of the FFT process, the DDRAM A and DDRAM B samples are replaced one-for-one by corresponding data samples from the EVEN/ODD working rams **118–130**, depending upon which ram bank is involved in the complex multiplication for a given symbol as discussed hereinabove. By replacing the carrier data of the previous data symbol stored in memory circuit **150** with the carrier data of the present data symbol stored in the working rams, the next data symbol is automatically prepared for the data demodulation process.

The final stage of the FFT algorithm accomplishes a second descrambling of the demodulated data symbol samples as shown by memory circuit 100_5. This second descrambling is an in-place combined descramble that prepares the demodulated data samples for input/output data exchange without a requirement of further buffering prior to a time de-interleaving process. As shown by memory circuit 100_5, the active demodulated carrier data points of the data symbol are again placed in the upper portions of the even and odd memory banks RAM A and RAM B (118–130). The second descramble thus places the symbol's data samples in time corrected order with respect to both of the EVEN and ODD memory banks, as shown by the resultant memory circuit 100_5, beginning with the even data samples 0, 2, 4, 6, . . . 6N/4–2 placed in the real locations, followed by the odd data samples 1, 3, 5, 7, . . . 6N/4–1 being placed in the imaginary locations, of the RAM A (RAM A EVEN 118 and RAM A ODD 126) or the RAM B (RAM B EVEN 122 and RAM B ODD 130) memory block, depending upon which of the ram banks is involved in the computation. The remaining locations of the EVEN and ODD ram banks are don't care conditions and correspond to the inactive carriers of the N-carrier system. The contents 100_5 of the working ram (memory circuit 100) thus represents demodulated data samples for a given data symbol that are appropriately ordered for subsequent processing by a time de-interleaving circuit, which contents are provided on signal path 52 (FIGS. 1 and 3).

While the invention has been illustrated and described in detail in the drawings and foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only the preferred embodiment has been shown and described and that all changes and modifications that come within the spirit of the invention are desired to be protected. For example, while the channel decoder circuit 35 of the present invention may be constructed of known discrete electrical components, circuit 35 is preferably formed of a single custom integrated circuit according to known semiconductor fabrication processes.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. Channel decoding circuitry comprising:

a first memory circuit having a first input for receiving and storing therein channel encoded digital data, a second input for receiving channel decoded digital data, and an output for producing the channel decoded digital data, the channel encoded digital data defined by a number of data symbols each including multiple adjacent data carriers phase modulated over time;

a second memory circuit having an input coupled to said first memory circuit output and an output, and holding channel encoded digital data of a previous data symbol therein;

a third memory circuit providing predefined calculation values at an output thereof; and

a multiplier circuit having a first input coupled to said first memory circuit output, a second input coupled to said second memory circuit output and to said third memory circuit output, and an output coupled to said second input of said first memory circuit, said multiplier circuit producing channel decoded digital data by complex multiplying corresponding data carriers provided by said first and second memory circuits along with said predefined calculation values provided by said third memory circuit, said first memory circuit simultaneously storing channel decoded data of a present data symbol provided by said multiplier circuit, producing channel decoded digital data of a previous data symbol at said first memory circuit output and replacing the channel decoded digital data of the previous data symbol with channel encoded digital data of a next data symbol.

2. The circuitry of claim 1 wherein the carriers of the channel encoded digital data are reversed in a time sequence thereof;

and wherein the carriers of the decoded digital data produced at said output of the multiplier circuit are provided to said second input of said first memory circuit in a corrected time sequence thereof.

3. The circuitry of claim 1 wherein said first memory circuit is partitioned into a first memory subcircuit and a second memory subcircuit, each of said first and second memory subcircuits alternately providing a present encoded digital data symbol to said second memory circuit and said multiplier circuit for decoding of the digital data while the other of said first and second memory subcircuits replaces a previous decoded digital data symbol with a next encoded digital data symbol.

4. The circuitry of claim 3 further including an address counter providing an address count at an output thereof;

and wherein each of said first and second memory subcircuits include an address input connected to said address counter output, said first and second memory subcircuits respectively storing and providing digital data samples in accordance with said address count.

5. The circuitry of claim 4 wherein each of said first and second memory subcircuits are partitioned into even and odd memory banks;

and wherein said even memory banks of said first and second memory subcircuits replace a previous decoded digital data symbol with a next encoded digital data symbol and said odd memory banks of said first and second memory subcircuits provide a present encoded digital data symbol to said second memory circuit and said multiplier circuit for decoding of the digital data if said address count is even, while said odd memory banks of said first and second memory subcircuits replace a previous decoded digital data symbol with a next encoded digital data symbol and said even memory banks of said first and second memory subcircuits provide a present encoded digital data symbol to said second memory circuit and said multiplier circuit for decoding of the digital data if said address count is odd.

6. The circuitry of claim 1 wherein the channel encoded digital data received at said first input of said first memory circuit is encoded in accordance with an inverse Fourier transform algorithm;

and wherein said multiplier circuit produces channel decoded digital data in accordance with a Fourier transform algorithm.

7. The circuitry of claim 4 wherein said Fourier transform algorithm includes one of a decimation-in-time radix-4 in-place Fourier transform calculation and a decimation-in-time split radix4–radix2 Fourier transform calculation.

8. The circuitry of claim 1 wherein the channel decoding circuitry is formed of a single integrated circuit.

9. Channel decoding circuitry comprising:

a first memory circuit having a first input for receiving and storing therein channel encoded digital data, a second input for receiving channel decoded digital data, and an output for producing the channel decoded digital data,

the channel encoded digital data defined by a number of data symbols each including multiple adjacent data carriers transmitted simultaneously over a predetermined frequency range, wherein each of the multiple data carriers are phase modulated over time;

a second memory circuit having an input coupled to said first memory circuit output and an output, and holding channel encoded digital data of a previous data symbol therein;

a third memory circuit providing predefined calculation values at an output thereof; and

a multiplier circuit having a first input coupled to said first memory circuit output, a second input coupled to said second memory circuit output and to said third memory circuit output, and an output coupled to said second input of said first memory circuit, said multiplier circuit producing channel decoded digital data by complex multiplying corresponding data carriers provided by said first and second memory circuits along with said predefined calculation values provided by said third memory circuit, said multiplier circuit further correcting for frequency offsets between data carrier frequencies of the encoded digital data and corresponding actual data carrier frequencies thereof by complex multiplying data carriers provided by said first memory circuit with said predefined calculation values.

10. The circuitry of claim **9** wherein said predefined calculation values include Fourier transform twiddle values.

11. The circuitry of claim **10** wherein said predefined calculation values further include accumulated linear phase rotation values for said data carriers.

12. The circuitry of claim **9** wherein the channel decoding circuitry is formed of a single integrated circuit.

* * * * *

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Ricci et al.

(10) **Patent No.: US 6,463,039 B1**
(45) **Date of Patent: Oct. 8, 2002**

(54) **METHOD AND APPARATUS FOR FULL DUPLEX SIDEBAND COMMUNICATION**

(75) Inventors: **Christopher P. Ricci**, Pembroke, MA (US); **William Peters**, Kingston, NH (US)

(73) Assignee: **Intelligent Ideation, Inc.**, Amesbury, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/065,838**

(22) Filed: **Apr. 24, 1998**

(51) **Int. Cl.**[7] **H04B 7/00**; H04B 1/68; H04Q 5/22

(52) **U.S. Cl.** **370/277**; 340/10.3; 340/10.4; 455/42; 455/46; 455/47

(58) **Field of Search** 370/276–277, 370/310; 375/219–221, 270, 301, 321; 455/42, 45–47; 340/10.1, 10.3, 10.34, 10.4, 10.41, 572.1, 572.2, 572.4, 572.5; 342/42, 44, 51, 410–414, 116

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Primary Examiner—Wellington Chin
Assistant Examiner—Maikhanh Tran
(74) *Attorney, Agent, or Firm*—Chris Ricci

(57) **ABSTRACT**

The invention is an apparatus and method for using electromagnetic energy as the means of automatic data collection (ADC). The communication system that comprises the invention utilizes frequency modulated ("FM") sideband electromagnetic energy to enable full duplex communication with another communication device. In one embodiment one of the communication devices is passive and the carrier is used to power the passive device. In another embodiment the communication devices are active and the carrier is suppressed to increase range or decrease power constraints, as the application requires.

18 Claims, 4 Drawing Sheets

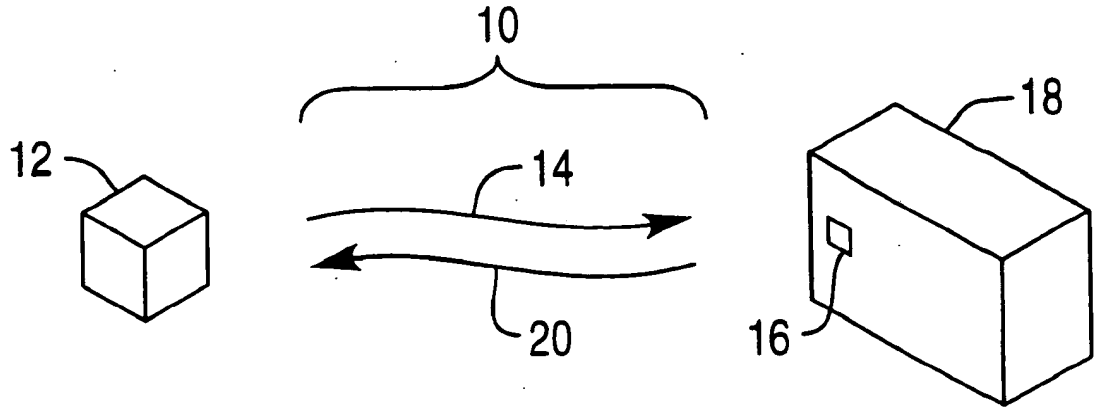


FIG. 1

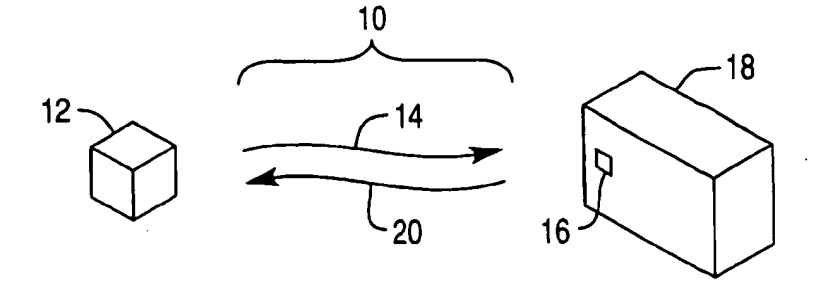


FIG. 2

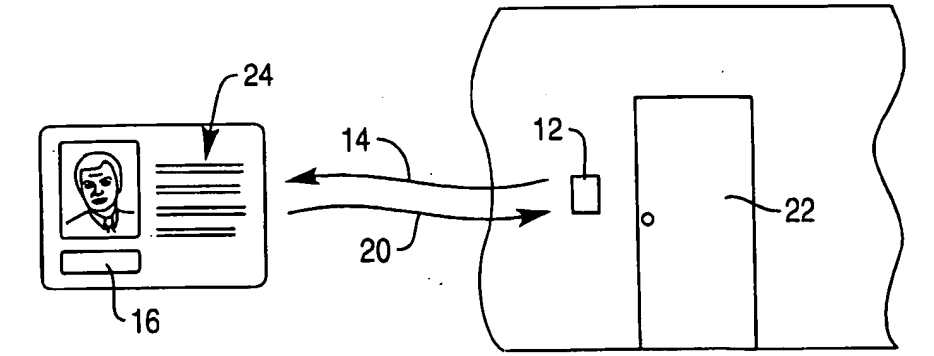
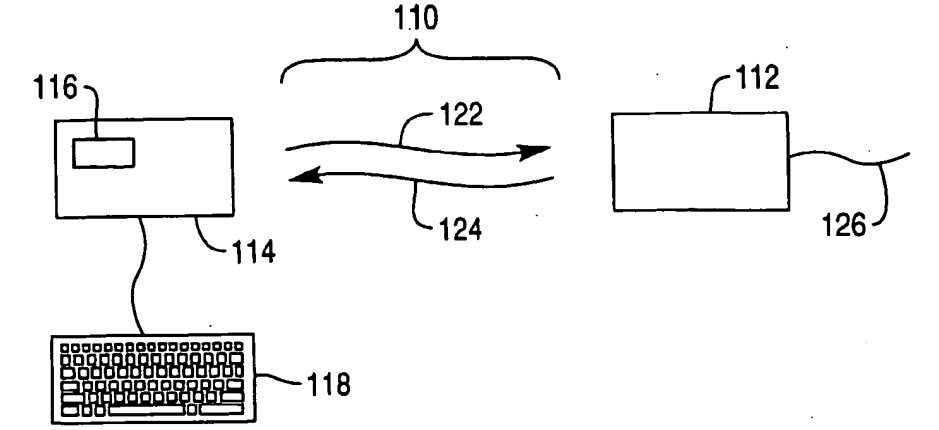


FIG. 8



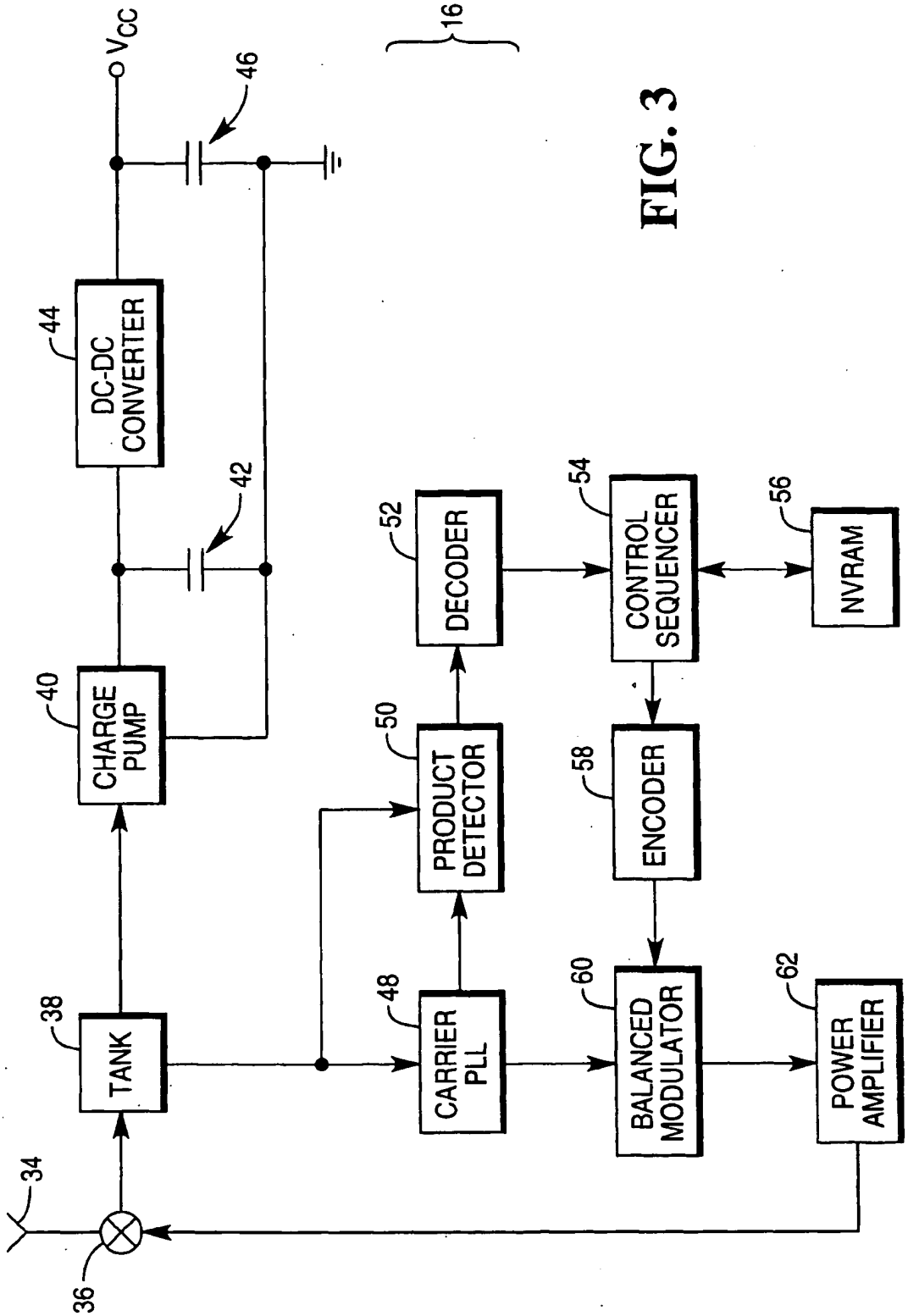

16
V_{CC}
46
44
DC-DC CONVERTER
42
40
CHARGE PUMP
38
TANK
34
36
48
CARRIER PLL
50
PRODUCT DETECTOR
52
DECODER
54
CONTROL SEQUENCER
56
NVRAM
58
ENCODER
60
BALANCED MODULATOR
62
POWER AMPLIFIER

FIG. 3

FIG. 4A

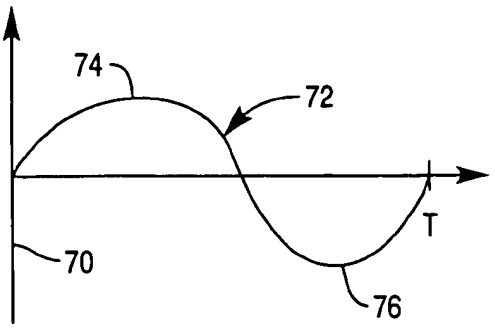


FIG. 4B

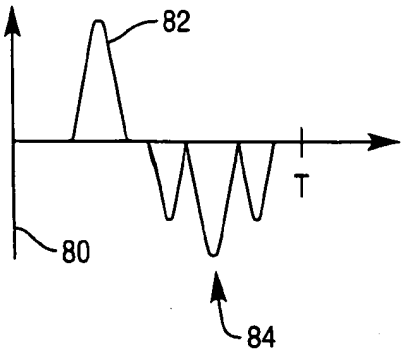


FIG. 5

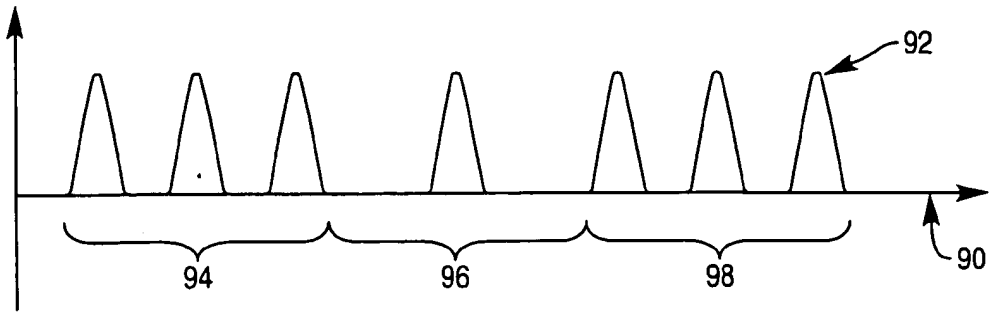


FIG. 6

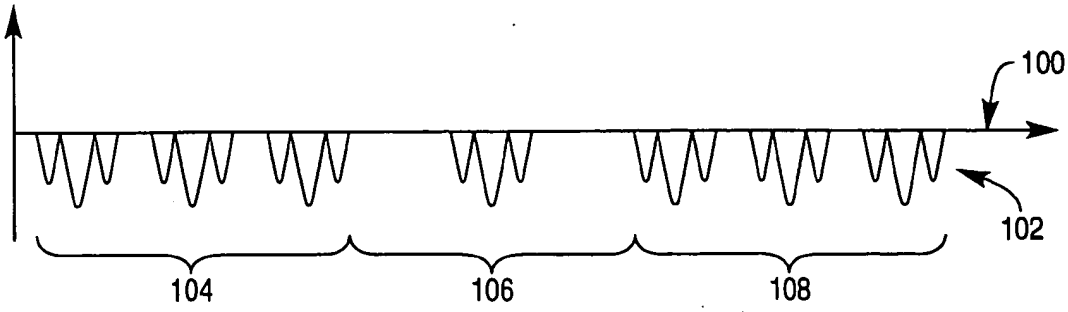
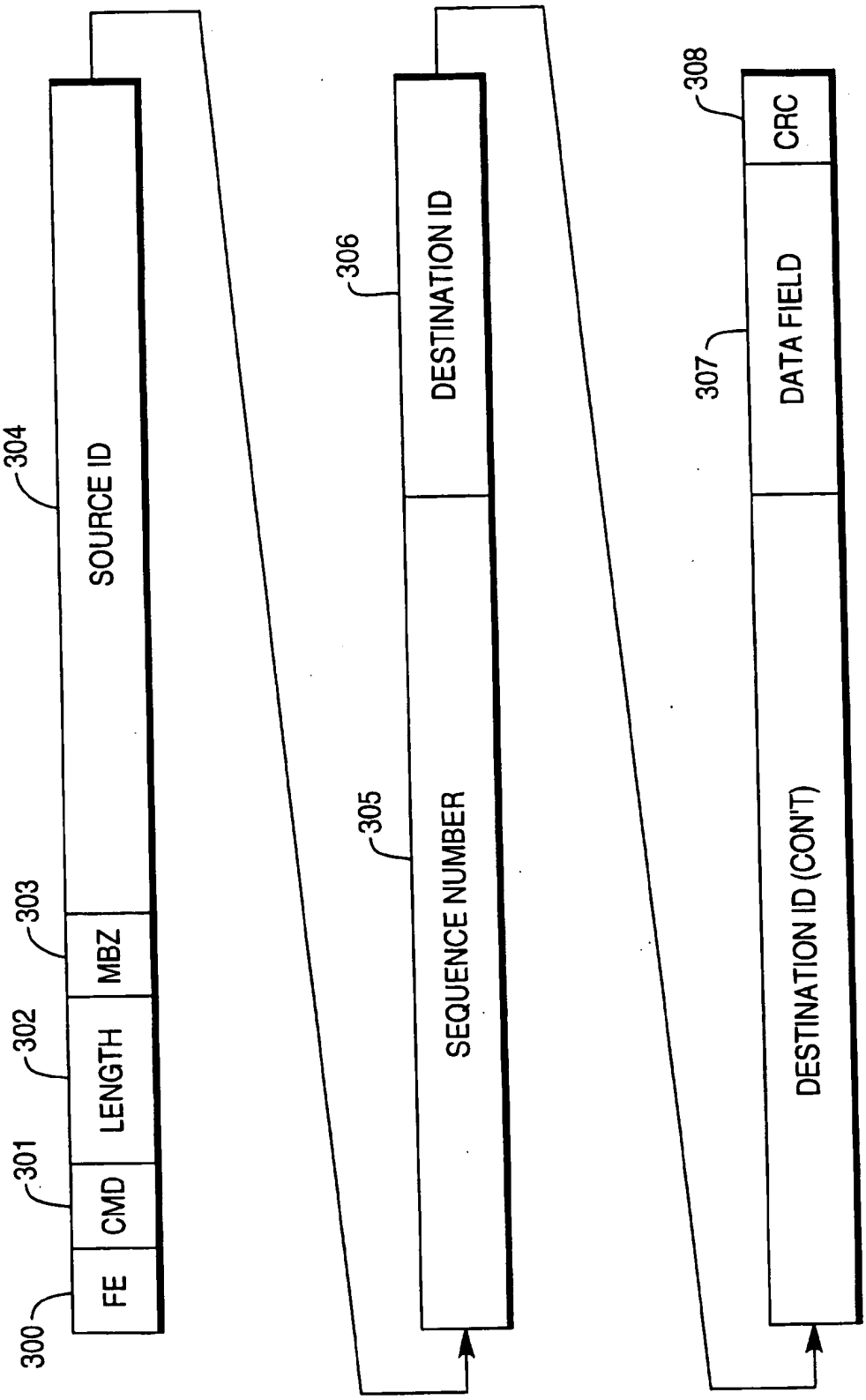


FIG. 7


300
FE
301
CMD
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LENGTH
303
MBZ
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SOURCE ID
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SEQUENCE NUMBER
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DESTINATION ID
307
DATA FIELD
308
CRC
DESTINATION ID (CON'T)

METHOD AND APPARATUS FOR FULL DUPLEX SIDEBAND COMMUNICATION

BACKGROUND OF THE INVENTION

The present invention relates generally to an apparatus and method for using electromagnetic energy as the means of automatic data collection (ADC). More particularly, the invention relates to an apparatus and method for using frequency modulated ("FM") sideband electromagnetic energy to enable full duplex communication with another communication device.

Radio frequency ("RF") remains the sole medium for conducting wireless communication. Despite the efforts of those in the fiber-optics industry to portray light as a wireless medium, it is still a materially bound, point-to-point connection that requires the use of cable.

In the RF domain, communication devices are further subdivided by their power source. The subdivision is generally based upon whether the communication device is "active" or "passive." An active communication device requires an external power source such as direct current ("DC") from a battery or alternating current ("AC") from a power grid, for example. In contrast, a passive device draws its power from ambient energy such as solar, wind, or ambient RF, for example.

Active devices have the most versatility due to their general lack of power constraints. However, in many applications an external power source is not practical. For example, in a vehicle navigation application where transponders are placed along a roadside, an AC connection to each transponder is cost prohibitive and a DC source causes severe maintenance problems.

Some of the many commercially active areas that are currently using passive wireless communications are Radio Frequency Identification ("RFID"), microcellular, and networking, for example.

RFID uses radio frequency transmission to identify, categorize, locate, and/or track people, animals, and objects. An RFID system is commonly composed of three components: an interrogator (reader), a transponder (tag), and a data processing system such as a computer.

The simplest form of RFID products can be compared to an electronic bar code. They operate by the interrogator transmitting a RF wave to the transponder. The transponder then absorbs the RF energy from the interrogator to change an internal power tank circuit. Sufficient energy is stored, the transponder transmits its stored code on a known frequency to be received by the interrogator. The data processing system then interprets the code.

More sophisticated RFID products interface with external sensors for measuring various parameters, including Global Positioning Systems ("GPS") which track objects. In these systems, the code transmitted by the transponder is variable.

One limitation to currently available RFID systems is that the interrogator and transponder communicate in an atomic sequence, i.e., one transponder at a time. The interrogator's RF field must be constrained to the general area expected to be occupied by the desired transponder. If two transponders are present, the read operation will fail.

In addition current RFID systems have the limitation that only one interrogator may acquire a transponder at any time. RF fields from closely adjacent interrogators will interfere with each others operation.

Further, even low levels of RF energy are very leaky and propagate into unexpected areas by unexpected means, commonly referred to as electromagnetic interference ("EMI"). Since the radio frequency spectrum is shared and busy, the interrogator/transponder communication channel is susceptible to disruption from random sources of RF. Therefore, current RFID technology relies on close proximity of the interrogator/transponder pair and exceedingly low power levels of operation to limit EMI. This has limited the art to a range of approximately one and one half meters maximum.

Sophisticated systems generally require an active system to support the required peripherals. Further, when used for tracking and locating, RFID remains expensive due to the extensive support peripherals required, such as GPS.

In microcellular applications, the current direction being explored is to use the harmonic generation and opto-electronic mixing properties of Mach-Zenhnder modulators to generate modulated subcarrier signals at high-order harmonics of the input signals. This permits the simultaneous transmission over optical fiber of a modulated and an unmodulated signal, both at high-order harmonic frequencies of the input signals, for the purpose of transmitting both a local oscillator tone and the modulated signal required at a base station for microcellular applications, see IEEE Transactions on Microwave Theory and Techniques, March 1996 v44 n3 p446(8).

Though this technique solves the problem of simultaneous communication of the modulated and unmodulated signals, it does so by constraining the transmission medium. Thus, this technique can not be applied to RF and even assuming that it could, it would require active devices on both ends.

In one commercially available system provided by RadioLAN, Inc., a RF networking card is used in a laptop computer to link the laptop to a local-area network ("LAN"). The transmission rate can be at 10 Mbps Ethernet speeds, but its use of proprietary protocols and non-standard narrowband frequency makes it useless in multi-vendor installations.

One approach that has been taken in the wireless industry has been the use of single-sideband transmission. In these systems, single-sideband is simply a sophisticated form of amplitude modulation. When RF and audio frequency ("AF") signals are combined in a standard amplitude modulation ("AM") transmitter (such as one used for commercial broadcasting) four output signals are generated: the original RF signal, called the carrier; the original AF signal; and two sidebands, whose frequencies are the sum and difference of the original RF and AF signals, and whose amplitudes are proportional to that of the original AF signal.

The sum component is called the upper sideband. The upper sideband is erect, in that increasing the frequency of the modulating audio signal causes a corresponding increase in the frequency of the RF output signal.

The difference component is called the lower sideband, and is inverted, meaning an increase in the modulating frequency results in a decrease in the output frequency.

All of the intelligence is contained in the sidebands, but two-thirds of the RF power is in the carrier. The carrier serves only to demodulate the signal in the receiver. If this carrier is suppressed in the transmitter and reinserted in the proper phase in the receiver, several significant communications advantages accrue. If the reinserted carrier is strong compared to the incoming double-sideband signal, exalted carrier reception is achieved in which distortion caused by frequency-selective fading is greatly reduced. Also, the lack of a transmitted carrier eliminates the heterodyne interfer-

ence common to adjacent AM signals. Perhaps the most important advantage of eliminating the carrier is that the overall efficiency of the transmitter is increased. The power consumed by the carrier can be put to better use in the sidebands.

In normal AM transmission, the power in the carrier is continuous and an AM transmitter requires a heavy-duty power supply. A double sideband transmitter having the same power output as an AM transmitter can use a much lighter power supply because the duty cycle is low. A single-sideband transmitter can, therefore, achieve the same effective range using one third of the output power as a standard AM transmitter.

A problem with AM is that it gives bursts of RF that are not always clear. Further, it is not as easy to detect shifts in an AM signal. This is particularly true with moving targets because amplitudes decrease proportionally to the distance to the transmitter.

Accordingly, it is an object of this invention to provide a wireless communication system that is adaptable to multiple applications.

It is another object of this invention to provide a wireless communication system that is power limited for passive applications.

It is still another object of this invention to provide a wireless communication system that is full duplex and can include unmodulated signals.

It is a further object of this invention to provide a wireless communication system that works in the presence of EMI, multiple transponders and/or interrogators.

It is still another object of the invention to use single-sideband transmission to increase range in passive RF systems but to do so without significantly decreasing the signal-to-noise ratio.

These and other objects of the invention will be obvious and will appear hereinafter.

SUMMARY

The aforementioned and other objects are achieved by the invention which provides a communication system and a method associated therewith. The communication system comprises a transmitter, a transponder, and a receiver.

The communication system described herein blends techniques in use by cellular and networked systems architectures into one. The protocol allows multiple RF targets and interrogators to coexist and function in a shared airspace through error handling and backoff algorithms similar to Ethernet. Thus completing a system for duplex data communications and simplified radio architecture.

The transmitter is adapted to transmit on a predetermined frequency a first sideband and adapted to have first frequency-modulated data encoded thereon.

The transponder then receives the first sideband and transmits on the predetermined frequency a second sideband disposed in a band distinct from the first sideband. The transponder is also adapted to have second frequency-modulated data encoded thereon.

The receiver then receives the second sideband on the predetermined frequency. The second frequency-modulated data is then decodable from the signal to complete the bi-directional communication.

In addition, the concentration of most of the RF power into natural sidebands and the reliability of FM propagation equates into greater operational range and design flexibility.

In further aspects, the invention provides methods in accord with the apparatus described above. The aforementioned and other aspects of the invention are evident in the drawings and in the description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects of this invention, the various features thereof, as well as the invention itself, may be more fully understood from the following description, when read together with the accompanying drawings in which:

FIG. **1** shows a block diagram of a communication system in accordance with the invention;

FIG. **2** shows a block diagram of a security system utilizing the communication system according to the invention of FIG. **1**;

FIG. **3** shows a block diagram of a transponder of the communication system of FIGS. **1** and **2**;

FIGS. **4**A and **4**B show graphs of a single cycle of a carrier wave and sidebands generated by the carrier wave, respectively;

FIG. **5** shows a graph plotting a pulse train of upper sideband pulses;

FIG. **6** shows a graph plotting a pulse train of lower sideband pulses;

FIG. **7** shows a data packet structure in accordance with the invention; and

FIG. **8** shows a block diagram of an active communication system in accordance with the invention.

DETAILED DESCRIPTION

While the present invention retains utility within a wide variety of communication devices and may be embodied in several different forms, it is advantageously employed in connection with communication devices having strict power limitations. Examples of such devices are passive devices that obtain power from a RF carrier or active devices that operate on batteries or require high bandwidth such that a standard RF channel is not practical. Though these are the forms of the preferred embodiments and will be described as such, these embodiments should be considered illustrative and not restrictive.

FIG. **1** shows a communication system **10** wherein an interrogator **12** transmits an interrogator signal **14** to a transponder **16**. In this embodiment, the transponder **16** is a passive device disposed on a package **18**. The transponder **16** identifies the package **18** thereby providing inventory control.

As is described more particularly in commonly assigned U.S. patent application Ser. No. 08/616,261 entitled "Vehicle Data Acquisition System" filed on Mar. 15, 1996, and incorporated herein by reference, the interrogator signal is used to provide power to the transponder **16**. One skilled in the art will realize however, that though the preferred embodiment draws energy from the carrier wave, solar cells, thermopiles, or other devices can be used to power the transponder in the passive embodiment.

The transponder **16** then encodes onto the interrogator signal **14** or copies the interrogator signal **14** and retransmits the copied signal with additional encoding. The transponder **16** encodes a code that provides information relative to the transponder **16**. That is, if the transponder **16** is attached to a package **18**, as is the case in this embodiment, the code would be indicative of the contents of the package **18**.

The encoded signal **20** is then transmitted back to the interrogator **12** where it is decoded.

This embodiment then allows for the reading of transponders located within a predetermined distance of the interrogator **12**. Thus, an interrogator can virtually instantaneously take a physical inventory in an entire room or track when and how a certain package was removed from inventory.

In another embodiment of the passive system, the transponder **16** is disposed on an identification card **24**. The interrogator **12** in this embodiment is used for security. The interrogator records the entry and exit of personnel through the door by reading the identity of personnel having the identification card **24**. The interrogator **12** can also be used to govern the lock on the door **22** so as to restrict access those having authorization.

This embodiment operates in a manner similar to that of the foregoing embodiment. The interrogator **12** transmits an interrogator signal **14** to the transponder **16**. In this case the transponder **16** is disposed on the identification card **24** which is worn by or otherwise located on a person. The transponder **16** encodes the interrogator signal **14** and returns an encoded signal **20** to the interrogator **12**. The interrogator **12** is loaded or otherwise electronically connected with an electronic database which determines whether that person has permission to enter. In higher security environments, a console may also bring up a photograph of the individual such that a guard can confirm that the holder of the indentification card **24** corresponds to the identification card **24**.

In this embodiment, single-sideband communication is used to accomplish the communication given the low power and/or high range requirements of the communication system.

The single-sideband communication used herein uses frequency modulation ("FM"). FM is free of many of the disadvantages of AM and, more particularly, is more resistant to noise and range limitations.

In this embodiment, two types of emissions are used in order to create a full-duplex communication path between the interrogator and the transponder. The interrogator transmits the upper sideband frequency products in the RF carrier frequency as well as the carrier signal itself, i.e., the carrier is not suppressed. Note that in conventional single-sideband operation the carrier is suppressed. However, the carrier in this embodiment is needed to energize the transponder and provide the initial frequency lock. The transponder then only transmits the lower sideband and suppresses its carrier to attain full-duplex communication.

This type of full-duplex communication allows the transponder to share a communication channel simultaneously with the interrogator allowing concurrent operations thereby substantially eliminating communication conflicts at the transponder. This also increases the effective radiated power of the transponder since all of the energy is being pumped into the information carrying frequencies and none is lost to the carrier or upper-sideband frequencies.

With any type of modulation technique and most kinds of encoding techniques the amount of information that can be transmitted on a channel is limited to one-half of its passband value. Whenever two frequencies are mixed, four frequencies result: the original two, the sum, and the difference frequencies. In the preferred embodiment, the passband is 80 kHz wide so the maximum deviation of the carrier frequency is 40 kHz above or below the center frequency, F_c.

Referring now to FIG. **3**, there is shown a block diagram illustrative of a transponder **16** of this embodiment. Like one of the previous transponder embodiments, a single antenna **34** is used for both reception and transmission. This can be accomplished substantially simultaneously owing to the single sideband transmission scheme employed where the upper sideband is used in one direction and the lower sideband is used in the other direction, thus providing full-duplex communication.

Additionally, coating can be used to increase signal strength passively. The coating must be such that it absorbs and/or amplifies ambient electromagnetic radiation. One example of such a coating is that manufactured by ARC Technologies, Inc., of Amesbury, Mass. One version of the aforementioned coating is described in U.S. Pat. No. 5,525,988 issued Jun. 11, 1996, entitled "Electromagnetic Radiation Absorbing Shroud." Though originally designed for use in radar avoidance systems such as that used in stealth aircraft, this coating amplifies the incoming signal before passing the signal to the antenna.

Following the path of an incoming signal, the signal is received by the antenna **34** and moved into a tank circuit **38** by a differentiator **36**. The differentiator **36** determines whether the signal is incoming or outgoing and routes the signal accordingly.

The tank circuit **38** is a passive tuned circuit designed to harness the power of the carrier signal. In the preferred embodiment, the tank circuit **38** has a center frequency of 924 MHz and a passband of 8 MHz. In one embodiment, the tank circuit **38** is implemented as a part of the antenna circuit **34** and is tuned by the placement and spacing of metal etch thereby eliminating a need for coils or tunable capacitors in the tank circuit **38**.

The tank circuit **38** passes the carrier signal on to a charge pump **40**. In the preferred embodiment, any signal in the frequency range of 920 to 928 MHz is determined to be a carrier signal for charging purposes.

The charge pump **40** is a voltage rectifier which rectifies the incoming RF signal from the tank circuit **38** and increases the signal voltage up to a useable direct current ("DC") level. In the preferred embodiment, this is a dual diode circuit. The output of the charge pump **40** varies depending on the strength (amplitude) of the RF input. In one sense, the charge pump **40** is an unregulated DC voltage source.

The DC output of the charge pump **40** is passed to a DC-DC converter **44**.

The DC-DC converter **44** is a regulation device designed to create a stable output voltage, V_{CC}. The output voltage, V_{CC}, is the power source for the remaining circuits in the transponder **16**. The DC-DC converter **44** is turned on when a threshold voltage is exceeded. In the preferred embodiment, the threshold voltage is 1.4 V and upon receiving this voltage or greater (within the operational range of the DC-DC converter **44**), a target voltage of 5.5 V for the output voltage V_{cc} is maintained. The DC operational range for the DC-DC converter **44** in the preferred embodiment is in the range of 1.4 V to 6 V.

An input energy storage device **42** and an output energy storage device **264** are used to store a sufficient amount of surplus energy to enable the transponder **16** to drive the RF power output for a predetermined amount of time. The predetermined amount of time will vary depending upon message length in the system which, in turn, will depend upon the application in which the communication structure is being used. In the preferred embodiment, the energy storage devices **42**, **264** are both capacitors and the predetermined amount of time is ten milliseconds.

Once output power V_{cc} is maintained, the remaining circuits are activated. The input signal, both the carrier and the upper sideband, is passed substantially simultaneously to a carrier PLL **48** and a product detector **50**.

The carrier PLL **48** has multiple functions. In the preferred embodiment, the carrier PLL **48** amplifies the incoming RF and bends it through a high-speed divider circuit internally. In the preferred embodiment, the high-speed divider circuit first divides the incoming RF by two and then again by three to obtain a frequency in the 154 MHz range suitable for use by high-speed digital logic. In another embodiment, this is accomplished using a local oscillator tuned to produce a difference signal having a frequency of 154 MHz when RF energy of a predetermined frequency is present. One advantage of the preferred embodiment over the latter embodiment is the elimination of traditionally bulky tuned circuits and the local oscillator.

The carrier PLL **48** uses a phase-lock loop ("PLL") to sense the center frequency of the incoming RF signal and lock on that frequency. The carrier PLL **48** provides a clock reference source for any derived frequencies in the transponder **16**, including digital clocks if necessary. In the preferred embodiment, the carrier PLL **48** locks on any frequency in the range of 153.33 to 154.66 MHz and a lock is achieved when a minimum of 100 cycles of RF energy is detected.

The product detector **50** is a FM discriminator which translates frequency variation in the received RF signal into a corresponding voltage waveform. The product detector **50** derives amplitude variations in response to frequency variations. In the preferred embodiment, the output of the product detector **50** has a peak voltage of 1.2 volts at the maximum frequency deviation (approximately F_C+40 kHz) and a null voltage of 0 V at the center frequency, F_c.

The output of the product detector **50** is a positive pulse train representing the two frequencies selected to perform the FSK by a decoder **52**.

The decoder **52** detects a shift in frequency of the pulses being received from the product detector **50** and produces either a digital 0 or 1. The lower frequency is sometimes referred to as a SPACE condition, while the upper frequency is sometimes referred to as a MARK condition. In the preferred embodiment, the SPACE condition generates a DC voltage of 3.3 V and represents a logical 0. A MARK condition shall generate a DC voltage of 0 V and represents a logical 1.

A control sequencer **54** is a state engine which decodes and implements the communication protocol of the transponder **16**. The control sequencer **54** frames the incoming digital data stream from the decoder **52** into a series of bytes, the meaning of which drives the next state sequence thereby determining the order of encoding in the output signal.

The control sequencer **54** also interfaces with an NVRAM **56**. In this embodiment, the NVRAM **56** is non-volatile random-access memory. The NVRAM **56** is used to store and retrieve variable information. Based upon the contents of the decoding, the control sequencer **54** decides which actions to take and which pieces of the information from NVRAM **56** should be encoded ad returned to the interrogator.

When the transponder **16** switches to transmit mode, the control sequencer **54** generates the digital data stream required by an encoder **58**.

The encoder **58** operates as described above for the decoder **52**, except in reverse. An input condition of SPACE generates the lower frequency and MARK generates the shifted frequency.

The encoded information is passed to a balanced modulator **60**. The balanced modulator **60** modulates the RF signal coming from the carrier PLL **48** with frequencies produced by the encoder **58**. To accomplish this, the balanced modulator **60** of the preferred embodiment uses a diode or field-effect transistor (FET) array. The result of the modulation process is an RF output signal in which the carrier frequency and all upper side band frequencies have been canceled or suppressed.

The RF output signal is then passed to a power amplifier **62**. The power amplifier **62** of the preferred embodiment is a class A type linear amplifier stage designed to raise the RF signal strength from the balanced modulator **60** to a level sufficient for transmission. In the preferred embodiment, the power amplifier **62** has a center frequency of 924 MHz and an 8 MHz passband.

The amplified output signal is then passed through the differentiator **36** and radiated out of the antenna **34** back to the interrogator.

Referring now to FIGS. **4**A and **4**B, there is shown a graph **70** illustrating a single cycle of a carrier wave **72** plotted on a voltage versus time scale. The carrier wave **72** has an upper half cycle **74** and a lower half cycle **76** and extends for a period, T.

As previously described with respect to AM, modulation of the carrier wave **72** causes the generation of sidebands **82**, **84**. Graph **80** illustrates that an upper sideband **82** is generated when the upper half cycle **74** of the carrier wave **72** is modulated and a lower sideband **84** is generated when the lower half cycle **76** of the carrier wave **72** is modulated.

To attain single sideband transmission in FM, only the upper half cycle **74** is modulated, thus generating only the upper sideband **82**. One skilled in the art will recognize that generation of the upper sideband may be accomplished in numerous ways, such as generating both sidebands and then suppressing the lower sideband, for example.

In the preferred embodiment, this is achieved by modulating the carrier only within a predetermined frequency range. For example, assume that the interrogator communication band is between 924.00 MHz to 924.02 MHz. FM operates by using an increasing frequency in the upper half cycle **74**, reaching the median frequency at the zero crossing and decreasing the frequency in the lower half cycle **76**. Thus, the upper half cycle **74** is modulated in this example between the frequency range of 924.01 MHz to 924.02 MHz. If modulation is clamped to only modulate the carrier signal **72** in this range then only the upper half cycle **74** is modulated and only the upper sideband **82** is generated.

In contrast to the conventional single sideband transmission, discussed above, the interrogator transmits the upper sideband **82** as well as the carrier signal **72**. The interrogator encodes information onto the upper sideband **82** while the carrier signal **72** provides both power and a clock reference to the transponder. Note that the interrogator is a powered device and, therefore, has minimal restrictions on power output (limited primarily by federal regulations) while the transponder, in the preferred embodiment, is a passive device that must maximize the usage of its power.

Origination information, such as that previously described, is encoded onto the upper sideband **82**. The data encoding technique is Frequency Shift Keying (FSK), although one skilled in the art will realize that Phase Shift Keying (PSK) or any of numerous other methods could also be employed.

In the preferred embodiment, the communication system is binary. A ZERO is defined as 23 kHz and a ONE is defined

as 26 kHz. This spacing provides both good key discrimination and a reasonable data rate. The actual choice of keying frequencies is application specific and any of numerous others could be used, however, the choice of frequencies does impact the FM sideband effect.

Unlike amplitude modulation which produces two distinct sidebands on either side of the carrier, frequency modulation produces an infinite number of sidebands on either side of the carrier. The amount of carrier power transferred to any set of sidebands is determined by the modulation index (M). The frequency deviation of the FM carrier has no relationship to the modulation frequency since the frequency deviation of the carrier represents the waveform or amplitude of the modulation information.

The modulation index is the maximum deviation divided by the modulation frequency. In the preferred embodiment, the modulation index is 1.7 which transfers maximum power into the first sideband. This also ensures that the power distribution facilitates transmission by making the first sideband twice as strong as the second sideband. The third sideband is very weak and the rest are nominal and thus be ignored. One skilled in the art will realize that adjustments to the index can be made to accommodate other design factors and, therefore, the invention can use a wide range of indices.

At other modulation indices, the design constraints of this embodiment are no longer achieved. For example, at M=2.405 substantially all of the carrier power appears in the sidebands. However, the second and third sidebands are nearly as powerful as the first and results in undesirable operation. At M equal to or less than 0.6, the sideband energies are not strong enough to create the desired effect.

The distribution of power to the sidebands for any given modulation index is calculated using Bessel functions, which are well-known in the art.

The maximum bit rate for this example is. Therefore. 40 K bits per second. With FSK data encoding, reliable detection of the frequency shift between logical zero and logical one requires several cycles of stability in the current condition. If 3 cycles per mark is allowed, the maximum data bit rate becomes 40K/3 or 13.3K bits per second. Since 10 bits are used to represent a single character with a 2 bit time intercharacter gap, the byte rate becomes 13.3K/12 or 1.1K bytes per second.

With some allowance for protocol overhead; the estimated data rate using FSK encoding is therefore equivalent to 9600 Baud. This data rate is adequate for many data acquisition systems given that the amount of data being sent is quite small. However, in other applications, other data rates can be achieved for more advanced encoding modes. For example, using 180 degree PSK, 28K baud can be achieved; using 90 degree PSK (QPSK), 56K baud can be achieved; using 45 degree PSK, 112K baud can be achieved; and, using Quadrature Amplitude Modulation+45 degree PSK, 448K baud can be achieved, for example.

Referring now to FIG. **5**, there is shown a pulse train **92** of upper sideband pulses on a graph **90** plotting voltage versus time. This pulse train has been frequency shift keyed to encode a binary message. In this example, A first group **94** has been frequency shifted to the higher frequency which indicates a logical one. A second group **96** has been frequency shifted to the lower frequency which indicates a logical zero. A third group **98** has been frequency shifted to the higher frequency which again indicates a logical one. Thus the pulse train **92** is decodable to be '101'.

Simultaneously transmitted from the interrogator with the pulse train **92** is the carrier signal. The carrier signal carriers power for charging the passive transponder and for providing a clock signal to the transponder circuit, both of which are described later herein. One skilled in the art will realize, however, that if the transponder has an independent power source or if the communication method is being used with another system not having such power constraints, then the carrier signal may be suppressed thereby increasing signal range or decreasing transmission power requirements of the transmitter.

Once the transponder receives the pulse train **92**, the transponder encodes its own message and sends the new encoded message back to the interrogator. Previously described was a method of accomplishing this task using a single carrier and mirroring that carrier back after adding additional modulation. In this embodiment, the transponder transfers the origination information encoded on the upper sideband into the lower sideband and follows the origination information with its own code. In the preferred embodiment, a predetermined protocol is used such that corrupted packets of information are known and rejected. The protocol is further used to order the information within the packets in a known way to facilitate decompilation.

FIG. **6** illustrates the encoding scheme of the transponder which mirrors that of the interrogator. A pulse train **102** of lower sideband pulses is shown on a graph **100** that plots voltage versus time. This pulse train **102** has been frequency shift keyed to encode a binary message. In this example, a first group **104** has been frequency shifted to the higher frequency which indicates a logical one. A second group **106** has been frequency shifted to the lower frequency which indicates a logical zero. A third group **108** has been frequency shifted to the higher frequency which again indicates a logical one. Thus the pulse train **102** is decodable to be '101'.

Since the encoding by the interrogator is on the upper sideband and the encoding by the transponder is on the lower sideband, bi-directional communication can occur substantially simultaneously in the same frequency spectrum without one transmission corrupting the other. Further, since the carrier no longer serves a purpose, the transponder suppresses the carrier and funnels the transmission power into the lower sideband thereby significantly increasing the range of the transmission.

A useful way of approximating the performance is to consider the theoretical isotropic point source antenna. All power radiated from such an antenna spreads out equally in all directions. Thus, a sphere of energy is radiated having a given surface area over which the energy is uniformly divided. The power available at any point in space is then inversely proportional to the area of the sphere. That is,

$$P_{eff}=P_{rad}/D2$$

where

P_{eff}=The effective power felt at the receiver;

P_{rad}=The effective radiated power from the transmitter;

D=Distance in meters.

The following is an example application of an application of the above equations to the previously described communication system. The assumptions used are purposely conservative and will vary in accordance with the application and its environment. The transponder is assumed, for example, to have high power requirements, though experiments have shown that this may not be the case.

In order to define a viable operating range, two main assumptions are being made: first, that the signal returned

from the passive transponder returns a minimum of 0.1 μW back to the reader antenna; and second, that the transponder will return all RF energy it receives less a twenty percent loss for internal efficiencies.

Using the above-stated functions and given a 1 Watt transmission, the transponder receives 10 mW at 10 meters and 2.5 mW at 20 meters. This is sufficient to generate 5 μW back at the interrogator. The stated minimum of 0.1 μW is reached at 30 meters.

Repeating this procedure with a 10 Watt emission yields 4 mW to the transponder at 50 meters. The energy delivered back to the interrogator is then 1.3 μW, above the minimum.

In practical applications, an isotropic radiation pattern does not exist. Therefore, assuming more realistic propagation patterns actual performance would likely be much better. In addition, these estimates are for pure radiation. The effects of modulation and, particularly sideband transmission, are not factored in. However, sideband transmission is estimated to increase the effective radiated power at the transponder by sixty-six percent and at the interrogator by thirty-three percent.

Referring now to FIG. **7**, a data packet structure is illustrated for use in implementing a communication protocol between the interrogator and the transponder. The following is a brief description of the fields and how they are used in the preferred embodiment. One skilled in the art will realize many alternative embodiments, but certainly a known protocol must be used for the state engine to understand what it is receiving and what it is expected to return.

The start character **300** signifies the beginning of a valid communications protocol packet. The start character **300** can be anything an implementor chooses. The preferred embodiment requires it be a hex "FE" character. When the interrogator begins transmitting, as previously described, the transponder is in a charging and synchronization phase. After a period of time, which is application dependent, the transponder is ready to receive a command packet. During this time the interrogator is transmitting a SPACE condition.

The command character **301** indicates what action is to be taken and also how various fields of the remaining packet are to be interpreted. A command character **301** has the following hex values and definitions in the preferred embodiment:

Command	Code	Description
BROADCAST	4A	Find any and all transponders in the area.
LOCATE_ID	4B	Find a specific transponder by identification
RESP_DATA	CA	Transponder read data response.
ACK_DATA	C1	Acknowledge good received data packet.
RETRY	CF or 4F	Retry last transmission.

All command characters **301** have bit **7** set to a 1 as an indication of a valid command character **301**. There are in addition two types of characters: command type characters and response type characters. A command type character always has bit **6** set to a 0 while a response type character always has bit **6** set to a 1.

The length characters **302** define the number of characters remaining to be sent in this packet not including the length characters **302**. The length characters **302** are transmitted as hex bytes MSB first, LSB last. The maximum length of the packet can be as little as 1 or as many as 65536 characters. In the preferred embodiment, the length characters **302** are two bytes.

The Must-Be-Zero character ("MBZ") **303** is used to indicate the end of the command header. A value other than zero in the MBZ **303** indicates a problem with the packet.

The source ID character **304** is the serial number of the interrogator as assigned on the date of manufacture. The combination of the source ID **304** and the sequence number **305** are used to uniquely identify a packet. In the preferred embodiment, each packet must transmit an acknowledged signal and thus this identification assists in the handling of collisions and other communications errors. In the preferred embodiment, the Source ID **304** is ten bytes.

The sequence number **305** is used to uniquely identify the current communication transaction. At first power on of the interrogator, the sequence number **305** is set to zero. Afterwards, when each successful transaction is completed the number is incremented by one. Overflow resets the number to zero. In the preferred embodiment, the sequence number **305** is ten bytes.

The sequence number **305** is used by the transponder state engine to keep track of command completion. When there are several transponders within range of an interrogator, all may be required (command dependant) to respond to the interrogator. A collision (two or more transponders transmitting at once) is a likely event. Each transponder stores the current sequence number **305** in the NVRAM along with a flag indicating completion. In this way the transponder will know to take no action if a duplicate command packet is received to which it has already responded. Interrogators will repeat the same sequence number in subsequent packets until all transponders have acknowledged the packet.

The destination ID field **306** is command specific and is used to address a specific transponder for specific operations. The destination ID is usually the serial number of the transponder as assigned on the date of manufacture. The destination ID field **306** is optional and in the preferred embodiment is fifteen bytes.

The data field **307** is command specific and may be used to pass parameters relative to the current command or in response packets is used by the transponder to return data requested by the interrogator. In the preferred embodiment data field **307** can range from zero to sixty-four kilobytes.

The CRC character **308** is the exclusive-or, or XOR, of each byte in the packet. The transponder calculates this value and compares it with the value of the CRC character **308** sent by the interrogator. If these values do not match, the packet is rejected and must be retried.

The above-described communication method is both useful in this radio-frequency identification system as well as various other applications. Any application having passive devices in the communication path can benefit but also those without such passive devices. By simply suppressing the carrier from the interrogator, bi-directional communication is achieved that is very resistant to noise, has relatively low power constraints, or, alternatively has a significant communication range. Examples of such applications are wireless networks such as LANs; walkie-talkies, though voice signals would generally have to be digitized prior to transmission; three-dimensional modeling and diagnostics for uses in areas such as robotics; inter alia.

FIG. **8** shows an alternative embodiment of the invention where the communication system is used with two active devices. Example of where this communication system is useful are low-power, high-bandwidth communication systems such as short-range video transmission; high data rate low error to noise ratio communications such as wireless LANs; and low-power high range systems such as microcellular. One skilled in the art will realize that the commu-

nication system is adaptable to numerous applications and, thus, is not limited to that described herein.

In this communication system **110**, a wireless LAN is shown where full-duplex communication is used and the carrier is suppressed to attain greater range at low power. In most cases, a hard-wired local area network ("LAN") **126** is already installed in a business environment. In that case, an interrogator **112** disposed in electrical communication with the LAN **126** and periodically transmits an interrogator signal **124**. The interrogator signal **124** communicates with a remote computer **114** having a transponder **116** disposed therein. In the preferred embodiment, the transponder **114** is disposed on an Ethernet card disposed in the remote computer **114**.

The remote computer **114** then encodes information in an encoded signal **122** which is transmitted back to the interrogator. The encoded information can be commands entered from a peripheral **118**, such as a keyboard, or any of various other devices.

In the active system, the transponder and the interrogator are interchangeable in that at any given time either can initiate communication with the other.

In the case of video communication, the video signal may be transmitted from the remote computer to a transponder. An example of a use for such a transmission would be to view the video on a television. In that case, the transponder would be electrically connected to a television and the video signal from the computer would be displayed thereon. A keyboard or mouse would then communicate with the transponder and the encoded signal would include information from those devices to control the remote computer.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A communication system comprising:

a transmitter adapted to transmit a first frequency-modulated data encoded on a first sideband of a predetermined frequency;

a transponder adapted to receive the encoded data on the first sideband and to transmit a second frequency-modulated data encoded on a second sideband of the predetermined frequency, wherein the second sideband is distinct from the first sideband; and

a receiver adapted to receive the second frequency-modulated data encoded on the second sideband transmitted from the transponder, and to decode the second frequency-modulated data therefrom.

2. The communication system according to claim **1** further comprising an interrogator in which the transmitter and the receiver are disposed.

3. The communication system according to claim **1** wherein the first frequency-modulated data is disposed within the second frequency-modulated data.

4. The communication system according to claim **1** wherein the transponder is passive.

5. The communication system according to claim **4** wherein the transmitter transmits a carrier signal from which and the transponder is adapted to draw energy from the carrier signal.

6. The communication system according to claim **4** wherein the transponder is adapted to draw energy from ambient radiation.

7. The communication system according to claim **1** wherein the first sideband is the upper sideband.

8. The communication system according to claim **1** wherein the second sideband is the lower sideband.

9. The communication system according to claim **1** wherein the communication system provides full-duplex communication.

10. The communication system according to claim **1** further comprising suppression means to suppress a carrier signal thereby augmenting transmission range.

11. The communication system according to claim **1** wherein the first frequency-modulated data is video.

12. The communication system according to claim **1** wherein the transponder further comprises an antenna and the antenna is coated with a radiation absorbing coating.

13. The communication system according to claim **1** wherein the transmitter transmits data using frequency modulation.

14. An interrogator comprising:

a transmitter adapted to transmit a signal on a predetermined frequency to a remote communication device which draws power from the signal;

a receiver adapted to receive a signal on a first frequency-modulated sideband of the predetermined frequency from the remote communication device; and

a decoder in electrical communication with the receiver for decoding information from the received signal,

wherein the transmitted signal is transmitted on a second frequency-modulated sideband of the predetermined frequency having a nondestructive relationship with the first frequency-modulated sideband and having frequency-modulated data encoded thereon.

15. A communication system comprising:

a first communication device having a first transmitter and a first receiver disposed therein, the first transmitter being adapted to transmit a first signal having first frequency-modulated data encoded on a first sideband, the first receiver being adapted to receive signal transmitted on a second sideband of the predetermined frequency and to decode second frequency-modulated data therefrom; and

a second communication device having a second receiver and a second transmitter disposed therein, the second receiver being adapted to receive signal transmitted on the first sideband of the predetermined frequency, the second transmitter being adapted to transmit on the second sideband a second signal having second frequency-modulated data encoded.

16. The communication system according to claim **15** wherein the first sideband and the second sideband have a nondestructive relationship.

17. The communication system according to claim **15** wherein the second frequency-modulated data comprises the first frequency-modulated data.

18. A method of radio frequency communication comprising the steps of:

transmitting a first signal having a carrier and a first sideband which is frequency modulated with origination information that identifies the source of the transmission;

drawing energy from the carrier sufficient to power a passive device;

encoding data onto a second sideband where the data comprises the origination information;

transmitting the encoded data on the second sideband;

receiving the encoded data on the second sideband; and

decoding the received encoded data.

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